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Optimization of ESD Protection Methods in Electronics Assembly Based on Process and Product Specific Risks

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Abstract

The last 40 years has seen significant development in electrical component and system technologies. However, advances with semiconductor technologies, cost optimizations, and die area shrinking have made electronics more sensitive to excess electrical stress and electromagnetic disturbances. In this dissertation work, one of these stress scenarios is studied: *electrostatic discharge* (ESD) risks in the electronics assembly process environment. In the assembly process, single electrical components, circuit boards, and different subassemblies are assembled together, tested, and programmed to complete fully functional electrical products.

A noncontrolled electronics assembly environment produces unpredictable ESD risks and causes yield losses. Therefore, it is necessary to protect electronics against ESD during handling and manufacturing. This is accomplished with the aid of an *electrostatic protected area* (EPA) and an ESD control program plan, which are typically built according to IEC61340-5-1-2007 and ANSI S20.20-2014 standards. These two standards define how to design, establish, implement, and maintain the program with administrative and technical requirements. Here, a 100 V *human body model* (HBM) limit is currently used as the base for building EPAs and ESD control programs. However, current ESD control programs are not always able to prevent ESD damages in EPA. On top of actual ESD events, there can be *electromagnetic interference* (EMI) initiated product and equipment disturbances in well-built EPAs.

In this research work, the main focus is on additional ESD control methods that go beyond the specifications and requirements of the IEC61340-5-1 and ANSI/ESD S20.20 standards. The objective is to optimize ESD protection methods based on real ESD risk scenarios found during PCB assembly, testing, handling, and during system final assembly to achieve close to zero-failure level. At the same time, the objective is to optimize ESD control-related costs in the process area.

Based on the research, the focus of the additional ESD and EMI control methods should be with final assembly, programming, and testing process phases where about 90% observed failure and disturbance cases have occurred. Therefore, in an improved ESD control program, EMI control, controlling product part and cable charging are added into the program, together with groundings and other basic controlled EPA items. The charging of product parts should be monitored with potential, discharge current and charge meters, and that data should be used together with process analysis to detect all known ESD risk scenarios. The sensitivity of subassemblies should be tested, for example, by using a *charged board event* (CBE), *field collapse event* (FCE), and *cable discharge event* (CDE) methods that simulate real world ESD scenarios found in the process area. This gives more accurate data for risk assessments than an electrical-component-specific HBM or *charged device model* (CDM) qualification data.

The proposed additional control methods were implemented in more than 10 large electronics assembly facilities, resulting in a significant reduction in ESD-related failures and disturbance-related process yield challenges. Therefore, as a future work, product and process specific ESD and EMI risk should be emphasized in ESD-control-related trainings, standards, standard practices, and technical reports.

Acknowledgments

This research work was carried out at the Department of Electronics and Communications Engineering, Tampere University of Technology, during the years 2013–2016. The research was not funded by external foundations, institutes, or companies. However, the research was supported by the NOKIA Corporation and Microsoft by sharing information and technical resources.

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List of abbreviations and definitions

AHE	automated handling equipment
CBE	charged board event
CDE	cable discharge event
CDM	charged-device model
DFMEA	design failure mode and effect analysis
DUT	device under test
FA	final assembly
FCE	field collapse event
FICBM	field induced charge board event
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPA	electrostatic protected area
EPS	external power supply
ESDS	electrostatic discharge sensitive device
EUT	equipment under test
HBM	human body model
HMM	human metal model
HV	high voltage
IC	integrated circuit
LGA	land grid array
LLP	lead less package
MFR	manufacturing failure rate
MM	machine model
OEM	original equipment manufacturer
PCB	printed circuit board
PWB	printed wiring board
ppm	parts per million
RF	radio frequency
RLC	resistance–inductance–capacitance
SCR	silicon controlled rectifier
SMD	surface mount device
SMT	surface mount technology
TLP	transmission line pulse
USB	universal serial bus

List of original publications

a. Tamminen P., Viheriäkoski T., Sydänheimo L., Ukkonen L., "ESD qualification data used as the basis for building electrostatic discharge protected areas," Volume 77, Journal of Electrostatics (2015), pp. 174-181.

b. Tamminen P., Ukkonen L., Sydänheimo L., "Correlation of component human body model and charged device model qualification levels with electrical failures in electronics assembly," Volume 79, Journal of Electrostatics (2015), pp. 38-44.

c. Tamminen P., Viheriäkoski T., "Product Specific ESD Risk Analysis," Paper 3B.2, EOS/ESD Symposium, 2011.

d. Tamminen P., Viheriäkoski T., Ukkonen L, Sydänheimo L., "ESD and Disturbance Cases in Electrostatic Protected Areas," Paper 5B.2, EOS/ESD Symposium 2015.

e. Tamminen, P., Viheriäkoski T., "Characterization of ESD risks in an assembly process by using component-level CDM withstand voltage," EOS/ESD Symposium, 29th, Page(s): 3B.3-1 - 3B.3-10, 2007.

f. Tamminen P., Viheriäkoski T., Reinvuo T., Sydänheimo L., Ukkonen L, "Field Collapse ESD Event," Paper 2B.2, EOS/ESD Symposium, 2014.

Related Publications

i. Paasi J., Tamminen P., Kalliohaka T., Kojo H., Tappura K., "ESD control tools for surface mount technology and final assembly lines," EOS/ESD Symposium, EOS-24, 2002.

ii. Paasi, J., Tamminen P., Salmela H., Leskinen J.-P., Viheriakoski T., "ESD control in automated placement process," EOS/ESD Symposium, 27th, Page(s): 1 – 9, 2005.

iii. Reinvuo T., Tarvainen T., Viheriakoski T., Tamminen P., "Electrostatic discharge measurement and simulation of a charged power amplifier board," Microwave Conference, 2009. EuMC 2009, Page(s): 292 – 294.

iv. Reinvuo T., Tamminen P., "Measurements and Simulations in Product Specific Risk Analysis," Paper 2B.2, EOS/ESD Symposium, 2011.

v. Viheriäkoski T., Peltoniemi T., Tamminen P., "Low Level Human Body Model," Paper 4A.3, EOS/ESD Symposium 2012.

vi. Viheriäkoski T., Tamminen P., Laajaniemi M., Kärjä E., Hillberg J., "Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials," Paper 2B.2, EOS/ESD Symposium, 2013.

vii. Tamminen P., et al., "ESD Sensitivity of 01005 Chip Resistors and Capacitors," Paper 9A.2, EOS/ESD Symposium, 2014.

viii. Smallwood J., Tamminen P., Viheriäkoski T., "Optimizing investment in ESD control," Paper 1B.1, EOS/ESD Symposium, 2014.

ix. Dunnihoo J., Tamminen P., Viheriäkoski T., "Near field EMC scanning method based on an E-field collapse method," International Symposium for Testing and Failure Analysis (ISTFA), USA, 2015.

x. Viheriäkoski T., Tamminen P., Peltoniemi T., "Comparison of Electric Charge Measurements," Paper 6B.3, EOS/ESD Factory Symposium 2015 and EOS/ESD Symposium, 2015.

xi. Tamminen P., Ukkonen L., Sydänheimo L., "The effect of USB ground cable and product dynamic capacitance on the ESD stress level with IEC61000-4-2 qualification," Paper 7B.2, EOS/ESD Symposium, 2015.

xii. Viheriäkoski T., Kohtamäki J., Peltoniemi T., Tamminen P., "Benchmarking of Factory Level ESD Control," Paper 6B.1, EOS/ESD Symposium, 2015.

Author's Contribution

This thesis includes two papers published in international peer-reviewed journals and four papers published in international peer-reviewed conferences. It also contains material from supplementary publications and some new unpublished results. The work presented here is the result of teamwork and analysis done during the last 15 years at VTT, NOKIA, Microsoft, and Tampere University of Technology.

For all the original publications, the author has been the first writer by completing a major part of the publication and carrying at least half of the data analysis, measurements, and simulations. With the publications [c], [d], [e], and [f], the measurements and analysis were made together with Mr. T. Viheriäkoski. With the related publications, the author has been the main contributor or participated in the analysis and paper writing process together with the co-authors. The role of authors Prof. L. Ukkonen and Prof. L. Sydänheimo has been advisory.

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1 Introduction

Electronics manufacturing consists of multiple parallel processes all targeted to produce electronic component and systems efficiently and with high quality. In this dissertation work, one of these processes is studied: *electrostatic discharge* (ESD) control, with the focus on optimization of subassembly and system-level ESD protection methods in electronics assembly. The background for the work was made between 2001–2005 at VTT, 2005–2012 at NOKIA Corporation operations and supplier network, during 2015 at Microsoft, and since 2012 at the Tampere University of Technology. This research work includes cooperation with about 20 large-size manufacturing facilities around the world, which produce a wide range of electronics from handheld consumer products to large-size industrial electronics. Here, an important role was with the NOKIA global ESD protection team consisting of ESD coordinators, technical, and laboratory services for electrostatic and ESD.

To guide the reader into the topic of the thesis, a short introduction to the ESD, ESD control, and ESD sensitivity of electronics shall be given.

1.1 Background

The need for ESD control was established after 1960s when solid-state electronics started to replace relay and tube technologies, and companies found that silicon- and germanium-based transistors, and diodes suddenly electrically failed during handling and processing. These new semiconductors also suffered more from electrical disturbances caused by fast transient electric events conducting or radiating electromagnetic pulses. This was a new kind of challenge — even electrostatics and visible sparking between metal electrodes had been known and studied extensively already several hundreds of years. Static-electricity-related risks also had been controlled in other industries and military already the mid-age to prevent ignition of gun powders and other flammable compounds. However, electronic components and systems had been robust so far, and tiny ESD sparks had not been formerly anything to worry too much about.

Throughout the 1960s–1980s, most electrical components were still able to withstand ESD stress measured in thousands of volts [1]. However, advances with semiconductor integration and introduction of *metal oxide semiconductor* (MOS) technologies during 1970s changed *integrated circuits* (IC) more sensitive to *electrical overstress* (EOS) and increased the need to test and qualify components against ESD in a more systematic way. There was also a need to measure and compare efficiency of different on-chip ESD protection structures inside the semiconductor devices. This information was used to estimate the required ESD control levels during component manufacturing, and also to inform system manufacturers how to handle electronic components in a safe way. For this purpose, companies used internal test methods mainly based on *human body model* (HBM) discharges [2]. HBM dates back to nineteenth century and was originally developed to study ignition risks of gas mixtures when a charged human discharges through a finger.

Most of the electronic components at that time were axial or radial through-hole type, until *surface mount technology* (SMT) became more popular during 1990s. Through-hole components were still assembled and soldered partially manually; therefore, HBM ESD scenarios were logically behind the first commonly used component-level ESD test standard MIL-STD-883, Method 3015.x published in 1980, which is the predecessor of the current joint JEDEC/ESDA standard JS-001-2014 [3][4].

It was also known that HBM was not able to represent all different real life ESD scenarios during single component handling. Therefore, additional component level test standards were created. A *machine model* (MM) simulates discharges from a charged equipment through the component into the electrical ground. A *charge device model* (CDM) is based on a scenario where an IC slides in a plastic carrying tube, gets a static charge by triboelectrification, and discharges into a grounded metal surface when it comes out from the tube. In this case, the source of the charge is the device itself. Currently, HBM and CDM are the main ESD qualification methods used with IC components [4]–[7][9]. MM test results overlap with HBM; therefore, JEDEC published a statement to discontinue the use of machine models for device ESD qualification [8][10].

The development of on-chip protection structures and systematic ESD safe handling procedures gave significant improvement to EOS/ESD-related risks between the 1980s and 1990s. The HBM withstand voltage of ICs was generally more than 2 kV HBM and CDM voltages more than 500 V. However, since the mid-1990s, component clock rates have exceeded GHz, the oxide thickness decreased close to 1 nanometer, and semiconductor wafer processes moved to sub 100 nm line widths. This prevented us from designing efficient EOS/ESD on-chip protection structures inside IC packages, and the safety margin between ESD safe handling processes and the sensitivity of ICs started to decrease [11]. One more limitation for the protection designs came from the area required for ESD protection versus the silicon area for active circuit functions. Therefore, generic on-chip immunity levels have decreased down to about 100 V – 1 kV from 2 kV HBM within the last 20 years. In addition, the decreasing gate oxide thickness has dropped CDM withstand voltages similarly, and, currently, ICs around 100 V HBM and 250 V CDM are commonly used in the industry.

During 1970s–1980s, electronic industry reported excess system and component failure levels during dry winter periods and, based on failure analysis, EOS and ESD were identified as the main suspects. To improve manufacturing yield, companies started to deploy ESD preventive actions independently, as there were not generic guidance or requirements available on how to do this. When the starting point of the ESD prevention in facilities was close to zero, the yield improvements and savings after protective actions were sometimes measured in millions of US dollars in a year [2][12]. This was also linked to the growth of the electronics industry, where a significant amount of industrial and consumer products were being made. One of the first protection methods taken into use were the grounding principles and the use of packaging materials with low charging and discharge shielding properties. This brought packaging material and personnel consumable and test equipment suppliers to work with ESD control and standardization activities. The early pioneer companies and institutes working with ESD protection methods and materials before 1980 were, to mention just a few, Charleswater Products Inc, USAF, NASA, IBM, General Electric Corporate, AT&T Bell Laboratories, Westinghouse Electric Corporation, RCA Corporation, Hewlett-Packard, Texas Instruments, and 3M Company.

When the knowledge of the ESD threads increased, the first EOS/ESD symposium was arranged by the companies and individuals interested in EOS/ESD control and design methods in 1979 in Denver, Colorado, USA [13]. The development of ESD control lead in USA to a military standard *MIL-STD-1686 - Electrostatic Discharge Control Program-1980* and a handbook *MIL-HDBK-263 - Electrostatic Discharge Control Handbook-1984*. These were the first documents commonly targeted to guide ESD control and are the direct predecessors of the current *ANSI/ESD S20.20* standard first published in 1999 [14]. In Europe, CENELEC published a standard *CECC 00015/1* in 1991, which was converted by the *International Electrotechnical Commission* (IEC) to a standard *EN100015-Protection of Electrostatic Sensitive Devices*, currently known as a standard *IEC61340-5-1* [15].

Currently, IEC and ANSI/ESD are the two main standardization bodies providing information for the electronics industry to measure and control ESD related risks. There are more than 200 different standards, standard test methods, technical reports, and guidelines providing tools for the ESD related process control and product qualification. The focus of these documents is with the next three generic phases of ESD control:

1. On-chip protection and qualification methods
2. IC and *printed circuit board* (PCB) manufacturing and handling
3. System assembly and qualification

1.2 Motivation

When creating the first ESD control programs for the electronics industry, the author took the technical requirements and the structure of the control process from the IEC61340-5-1-x and ANSI S20.20-x standards [14][15]. Both these standards use the HBM 100 V as a base to build up an *electrostatic protected area* (EPA) and ESD control programs. The latest version of the ANSI/ESD S20.20-2014 has now also an additional 200 V CDM and 35 V on isolated conductor target values. However, there were questions as to what to improve or control more when more sensitive electronics would be handled, and both the HBM and CDM withstand voltages would decrease. This pushed us to study more about how HBM and CDM qualification methods are built and how to use the withstand voltage information to improve ESD control methods in EPAs. There were also questions

about how decreasing withstand voltages would affect system designs and qualification and how to use sensitive components in a system without major EMC/ESD design challenges and field failures.

When going through the HBM and CDM qualification methods, it became more evident that IC qualification data given as the withstand voltage would be challenging to use to assess the effectiveness of ESD control in EPA. In addition, the system-level qualification information based on the IEC61000-4-2 standard had challenges to represent the sensitivity of subassemblies handled in electronics assembly [16]. There were also several major ESD failure cases and new ESD risk scenarios found in modern automated electronics manufacturing, which were not fully covered by the control programs following the standards. This initiated research tasks targeting to define more exact target levels to estimate the real ESD risks in different production and handling steps. One more motivation was to optimize the control process so that cost of ESD protection would decrease and that the EPA would not limit the sensitivity of components or subassemblies used in products. Thereby, the sensitivity of used components would be defined by the system design phase, and all later operations would be aligned based on the tested ESD risk scenarios. All these additional targets would be built on top of an existing ESD control in an electronics assembly facilities.

1.3 Objectives and Scope

This thesis has its main focus on the advanced ESD control methods in electronics assembly operations that go beyond the specifications and requirements of IEC61340-5-1 and ANSI/ESD S20.20 standards. The objective is to optimize ESD protection methods based on the real ESD risk scenarios found during PCB assembly, testing, handling, and during system final assembly in EPA environment to achieve close to zero failure level.

The scope of the research starts from automated surface mount assembly lines, where all the single ICs are assembled. A *printed wiring board* (PWB) testing phase is the next, followed by a system assembly and final testing. Product and process-specific ESD control methods are presented together with the subassembly ESD sensitivity analysis. Thereby, these methods are applied to electronics manufacturing operations where ESD sensitive components and subassemblies are handled. The main research questions are

- Can we use the IC level HBM and CDM qualification data to optimize ESD control in electronics assembly?
- Can an on-chip, on-board, and system level EMC/ESD protection designs prevent ESD failures in electronics assembly processes?
- Where do most of the ESD failures occur and what is the type of failure events in electronics assembly?
- What additional control methods shall be required on top of the current standard practices?
- How do we implement these additional control methods?

1.4 Structure of the Thesis

This dissertation is based on six publications, denoted [a]–[f] and is also supported by the author's publications [*i*]–[*xii*]. The scientific contribution of these publications are discussed in the author's contribution section. References are cited with Arabic numbers. The structure of the thesis is illustrated in Figure 1.

Chapter 1 gives an introduction, background, and motivation for the thesis. It will shortly explain the main motivation to construct and specify ESD protected areas and introduces current standards to build up ESD control programs.

Chapter 2 introduces the target environment, electronics assembly, which includes process phases from components placement up to a final assembly and testing.

Chapter 3 provides the theoretical background for electrostatic discharge events and explains how the resulting transient current–voltage waveforms can be calculated in a time domain with basic mathematical methods. The chapter will also discuss the electrical component failures ESD waveforms can produce, thus, giving information to detect ESD risk in an electronics assembly.

Chapter 4 goes through protection techniques with electronic designs. These are based on on-chip designs inside IC packages, on-board protection components on the PCBs, and system-level protection design methods. In addition, the chapter introduces component, subassembly, and system-level ESD qualification and testing methods and discusses how these could be used to assess real world risks in electronics assembly environment.

Chapter 5 discusses different ESD risks in electronics assembly. ESD and electronics disturbance risks found in EPAs are analyzed to provide information for the additional required control methods.

Chapter 6 presents the additional control methods. The focus is on the most severe process phases and risk scenarios in electronics assembly.

Finally, Chapters 7 and 8 have the discussion and conclusion of the thesis.

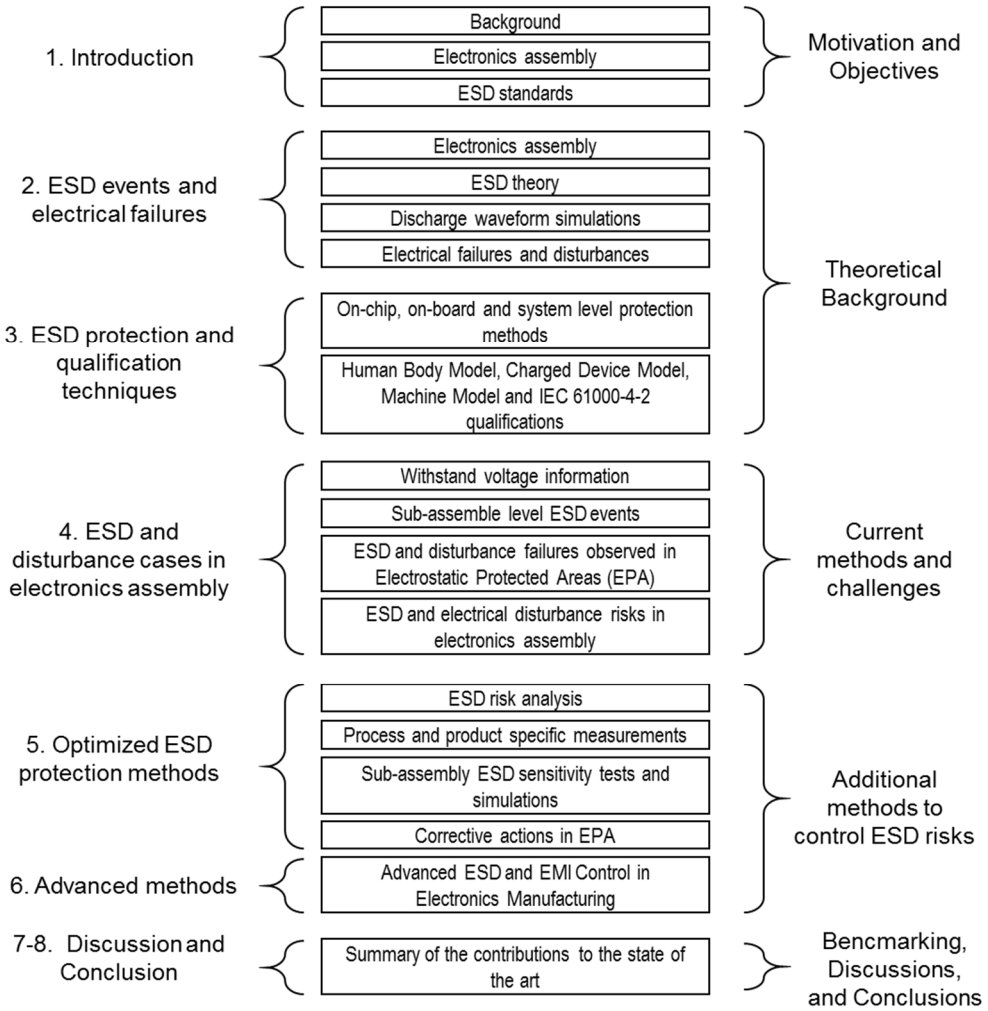

Figure 1. Structure and contents of the thesis.

2 Electronics Assembly Processes

An electronics assembly environment can be built in different layout formats depending on the scale of production and type of the products under manufacturing. However, most of the process phases are similar between facilities, and, to simplify the analysis, the assembly process is described here as a continuous line with connected process phases, as shown in Figure 2. A *surface mount device* (SMD) assembly process typically contains the following phases: paste printing, component assembly, conveyors, PCB buffers, soldering, and testing, as shown in Figure 3. After the PWB assembly, there can be several parallel and serial *final assembly* (FA) phases, programming, testing, and packaging phases, as shown in Figure 3 and Figure 5. An FA can also get completed PWBs, subassemblies, and modules from other facilities, and only part of the assembly and final testing will be completed in one specific process area. In addition, it is common to run the FA process in separate parallel cells working independently of each other. This FA format is more flexible, can produce simultaneously different products, and can tolerate better production volume changes.

SMD operations are nowadays completely automatized, and operators do not typically touch on single ICs or PCBs. There is much more variation with FA processes where assembly operations can be made manually, with robots, or by combining manual and automatized process phases. Similarly, testing and programming can vary from a manual to fully automated process. Most contacts with electronics are made by assembled subassemblies, process equipment, test connectors, and tools used in the process area. All these processes need to be part of an EPA where an ESD control program is running. There are also typically more workers operating in FA, testing, and packaging areas than in the SMD process. All they need to follow ESD protective precautions where dissipative shoes and wrist traps are the main ESD protection methods by providing a ground path for static charges.

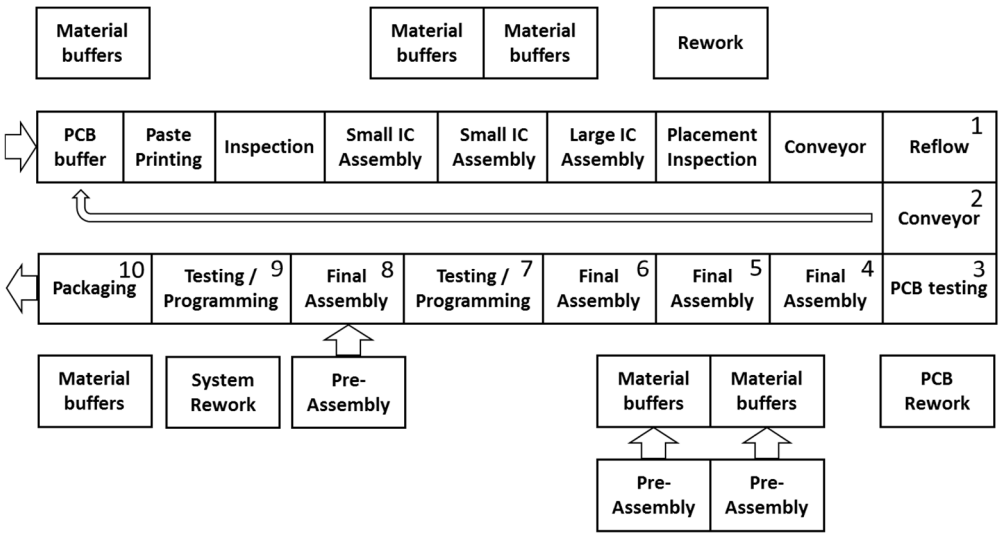

Figure 2. An example layout of a single electronics assembly line with SMD, FA, testing, and programming processes.

Wave soldering, manual soldering, and press fit connectors are still common processes in electronics assembly. Large-size electrical components, such as through-hole transformer joints and electrolyte capacitors, cannot be soldered in a reflow process. In addition, rework phase may use manual soldering tools or a specific component replacement equipment with an optical alignment for *ball grid array* (BGA), *lead less package* (LLP), and *land grid array* (LGA) components. However, it is not common to hand solder ICs anymore as a pin spacing is typically between 0.3 and 1.27 mm and BGA type of ICs have the joints hidden under the package.

Testing and programming phases vary largely, depending on the type of the products. Electrical testing or programming can be done with pin-bed in-circuit testers, via specific test interface connectors and via product user interface connectors, such as *universal serial bus* (USB) ports. In addition, part of testing and programming can be made via radio links if the product has a functional software and a power supply available. Products with

radio communication features require sophisticated RF testers for Bluetooth, GSM, LTE, WLAN, GPS, and other possible connection protocols. Products with a display and other visual or audial functions may require additional inspection tools: for example, for cameras, microphones, touch screen and keyboard pressing tools, and magnetic sensors.

Different programming and testing phases can also be integrated into one process phase, thus, testing and programming equipment can be complex systems with demanding software applications and robot manipulators in place. This equipment is often process and product specific with changeable tools, jigs, and adapters. System-level functional testing is still commonly made manually, as a human can make different tests and inspection tasks without hardware changes or demanding programming tasks.

The speed of the assembly operations can vary largely depending on the type of the products and processes. In a fast process, such as in a component assembly, one assembly operation can take less than 0.1 s, whereas wave or reflow soldering, product testing, and programming can take from a few seconds up to tens of minutes per product.

Mechanical and electrical components are typically kept in plastic packages or on trays until assembly, as shown in Figure 4 and Figure 5. These packages can be made of static dissipative or dielectric material, depending on the type and ESD sensitivity of the part. The packages can also have moisture barriers and discharge shielding properties.

Figure 3. An SMD process area with several parallel assembly lines.

Figure 4. A part of semi-automatic FA line with a flat belt conveyor.

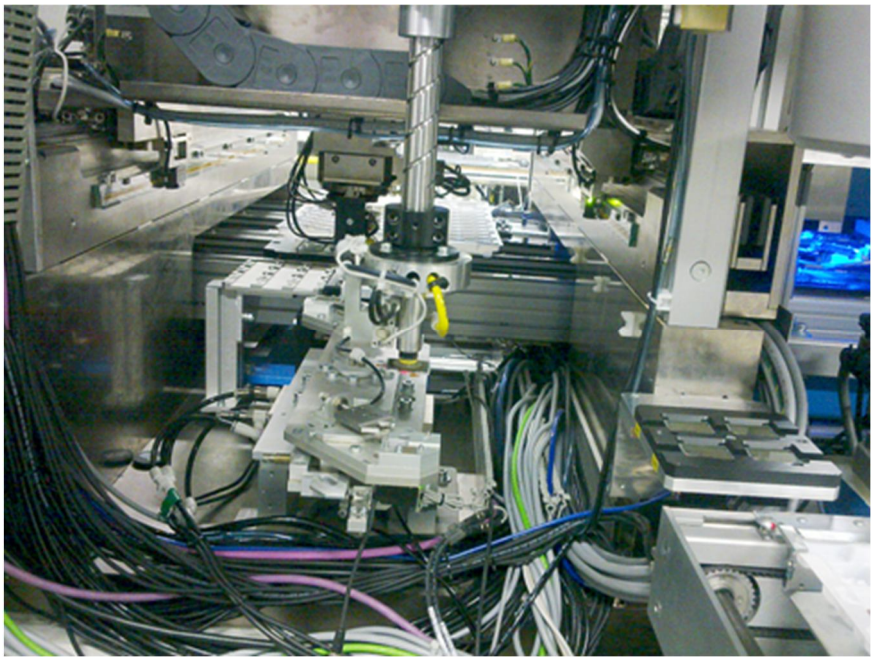

Figure 5. An FA robot cell with pickup tools and automated material loading.

3 Electrostatic Discharge Event

3.1 Discharge Current Waveforms

A destructive electrostatic discharge event in electronics manufacturing occurs in most cases between two conductors with different potential levels. ESD occurs when the conductors approach each other and an *electrostatic field* (E-field) breakdown occurs through the dielectric volume. In a normal air pressure, the E-field breakdown takes place around 3 kV/mm depending on the shape and size of the objects, but, if the potential difference is below the Paschen limit, the discharge may occur only when the objects come into contact with each other [17]. During the ESD event, charge carriers flow between the two objects and equalizes the potential difference. The amount of maximum charge moving Q_{Mobile} depends on the potential $V_{Initial}$ and capacitance C_{Source} based on equation (1). When the objects are not grounded, the amount of charge moving depends on the voltage difference and capacitance of the objects before the discharge. It is also possible to get a discharge with several amperes peak current from a surface of an insulator with a high surface charge density. However, these discharges less likely cause electrical failures with non-grounded components as the discharge current amplitudes are typically at mA level, and there is a limited total charge transfer from the dielectric surface [18].

$$Q_{Mobile} = C_{Source} V_{Initial} \quad (1)$$

Before an ESD event, potential energy is stored in the electrostatic field of the discharge source capacitance C_{Source}. This field can be, for example, between a charged metal object and electrical ground. The voltage on the charged object is not constant if the physical position of the object changes because the source capacitance depends on size, shape, and distance of the charged object to the environment. However, the charge Q_{Mobile} is a constant—as long as there is no current leakage from the object. Therefore, the voltage $V_{Initial}$ and charge Q_{Mobile} at the moment of the ESD event defines the amount of energy released during the discharge event based on equation (2). The charge of the object can also be polarized by an external electrostatic field. In that case, the potential of the object depends on the density of the electrostatic field, shape of the object, and position of the object between the ground reference plane and the source of the electric field.

$$E = \frac{1}{2} Q_{Mobile} V_{Initial} = \frac{1}{2} C_{Source} V_{Initial}^2 \quad (2)$$

Before the ESD event, the initial voltage and charge values are quasi-static, but, when the discharge channel opens, the quasi-static event changes to an RF event taking place around nanoseconds period. Figure 6 shows a simplified serial *resistance–inductance–capacitance* (RLC) equivalent circuit for a discharge event. The source resistance R_{Source} has a high >1 MΩ value to charge the capacitance C_{Source} up to the initial potential level V_0. When the capacitor is fully charged, the switch closes, and the capacitor discharges via an inductance L and a resistor R_{DUT}. The R_{DUT} represents an ESD sensitive electronic device with an internal resistance burning the energy of the discharge current. Therefore, the most interesting parameter to monitor in an ESD event is the current *i(t)* flowing through the sensitive component.

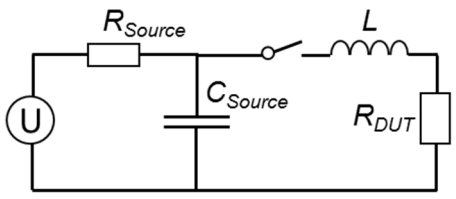

Figure 6. Discharge RLC circuit

In Figure 6, the discharge starts when the switch closes and the potential difference starts to equalize through the RLC circuit. A two-pole RLC model current waveform can be expressed in the s-domain by using a voltage step pulse $V(s) \approx V_{0/S}$ as an input and using Laplace transforms [19]. Similarly, discharge current waveforms can be modelled by using a step function in the RLC circuit with an initial voltage V_0. Based on Kirchhoff's voltage law, the sum of voltages across the resistor, inductance, and capacitance equals with the source voltage in a serial RLC circuit. In a time domain, the current equation can be expressed as

$$\frac{d^2i(t)}{dt^2} + 2\alpha\frac{di(t)}{dt} + \omega_0^2 i(t) = 0, \qquad (3)$$

where $\alpha=R/2L$ and $\omega_0=1/(LC)^{0.5}$.

For the underdamped current step response, we can write

$$i(t) = Ne^{-\alpha t}\sin(\omega t + \varphi), \qquad (4)$$

where $\omega = \sqrt{\omega^2{}_0 - \alpha^2}$.

The arbitrary constant N and the phase shift φ can be solved from the initial boundary conditions. For a charged object, the initial voltage is V_0, and the current flow is zero. The square root has three different solutions depending on the RLC values. The current waveform is underdamped if $R^2<4L/C$, overdamped if $R^2>4L/C$, and critically damped when $R^2=4L/C$ [20].

Therefore, for the underdamped current step response, we can write

$$\mathrm{i(t)} = \frac{\mathrm{V_0}}{\mathrm{L\omega}}\mathrm{e}^{-(\frac{tR}{2L})}\sin(\omega t), \qquad (5)$$

where $\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$.

For the overdamped current step response, we can write

$$i(t) = \frac{\mathrm{V_0}}{\mathrm{L\omega}}\mathrm{e}^{-(\frac{tR}{2L})}\sinh(\omega t), \qquad (6)$$

where $\omega = \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$.

Finally, for the critically damped current step response, we can write

$$i(t) = \frac{\mathrm{V_0}t}{\mathrm{L}}\mathrm{e}^{-(\frac{tR}{2L})}. \qquad (7)$$

Equations (5), (6), and (7) represent ideal step responses, but, during an ESD event, discharge path parameters can vary. Especially, the serial resistance R can vary due to changes in the spark plasma channel and an adiabatic heating of objects along to the current path. In addition, there can be several parallel source circuits taking part to the same ESD event. Figure 7 shows example waveforms based on equations (5) and (6), where the *sum of waveforms* is a sum of underdamped and overdamped ESD pulses. The resulting sum waveform is a typical response of a discharge event from a small charged object with parallel inductive and resistive paths, such as a PCB with multiple traces, ICs, and power planes. In this case, there are both an overdamped 100 Ω path and an underdamped 20 Ω path with 20 nH inductance forming the sum waveform. Naturally, more than two sinusoidal functions with attenuation parameters can be summed together to get an even more accurate waveform estimation. In addition, in real life, there is typically current and voltage signal reflections due to an impedance mismatch between the source circuit and *device under test* (DUT). These reflections can play a significant role with ESDS failing thresholds and need to be under control when electronics components and systems are qualified against ESD [20][21][26]–[29].

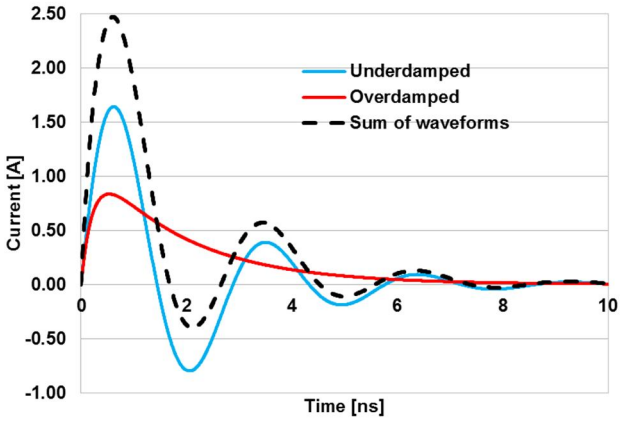

Figure 7. Ideal discharge waveforms.

3.2 Electrical Component Failures Due to ESD

ESD events can produce different damage for electronics depending on the rise time, amplitude, oscillation frequency, and length of the discharge current waveform. One way to describe the failure mechanisms was presented by Wunsch-Bell and Dwyer, where the failure power and energy of semiconductor devices depends on the amplitude and width of the pulse [22][23]. In order to damage electronic devices with short pulses, the required peak power or energy follows the *1/t* relationship, as shown in Figure 8. In this adiabatic region, the heat has no time to spread, and the damage signature is typically local. When the length of the pulse expands to a non-adiabatic region, heat starts to spread to the close environment, and the required failure power and energy follows more the *1/log(t)* or $1/t^{0.5}$ relationships. Finally, with long pulses, an equilibrium state is reached (noted as *C* in Figure 8).

A dielectric breakdown failure occurs when an electrostatic field exceeds a breakdown limit of an insulator. The insulator can be a gas or a dielectric material, such as a *silicon oxide* (SiO2) or high-k hafnium dioxide in a transistor gate. SiO2 has the dielectric breakdown strength around 1000 V/µm, but modern transistors may have the dielectric thickness from below 1 nm up to a tens of nanometers, and the resulting breakdown voltage can be as low as 0.5 volts [21][24]. However, a maximum quasi-static voltage or E-field rating of the oxide may not apply to fast transient events if the charge of the event is not high enough to cause permanent damage. Several cumulative pulses can still be able to destroy the dielectric and produce a conductive path through the dielectric, thus producing a leakage current [vii].

The required pulse length for each failure region depends on the size and type of the electronic device. Most on-board protection components are in the non-adiabatic region due to the higher energy dissipation capability, but small size semiconductor designs can get failures already with a less than nanosecond long current pulse width [23]. However, in reality, ESD pulses are seldom rectangular shaped, and the power–energy failure behavior model should be applied separately to different parts of the pulse. For example, a current pulse with a very fast rise time can trigger non-adiabatic failures, even if the total pulse length is more than 100 ns. In that case, the speed of current change and the inductance along the current path on a sensitive area of a silicon induces an excess potential difference based on equation $V_\Delta = L\frac{di}{dt}$. The voltage V_Δ can exceed a dielectric breakdown strength on the silicon and cause physical damage [21].

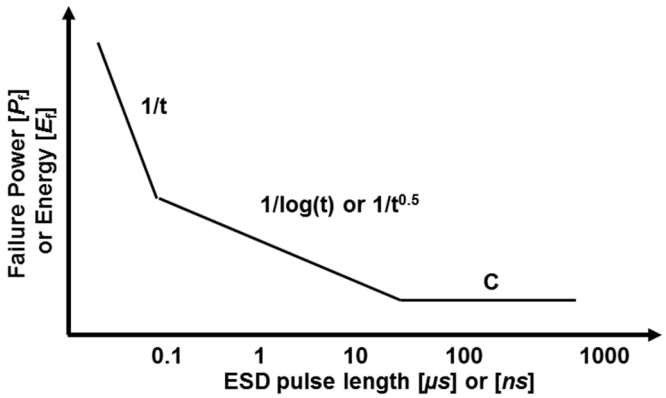

Figure 8. Wunsch-Bell-Dwyer pulse length versus power–energy failure levels.

There are several methods to calculate the required discharge energy and power failure limits. The total energy of a discharge can be calculated based on equations (2) and (8). In case the energy or power should be calculated in a certain part of the pulse, equations (8)–(11) can be used. The energy burns into heat in resistive loads along the discharge path based on power equations (10) and (11).

$$E = \int_m^n P(t)dt \quad (8) \qquad Q = \int_m^n i(t)dt \quad (9)$$

$$P(t) = i^2(t)R = \frac{V^2(t)}{R} \quad (10)$$

$$P = vi = \frac{1}{2}V_p I_p \cos\theta \quad (11)$$

In equations (8)–(11), Q is the transferred charge, V is the initial discharge potential, C is the source capacitance, E is the transferred energy, P is the power, θ is the phase between current and voltage, R is the resistance, and i is the current of the discharge waveform. Figure 9 shows total power and energy curves of the current waveforms shown in Figure 7. The highest peak power follows the peak current waveform, whereas the energy is an integral of the total power curve. In this case, the damage could occur either due to the peak power around 1 ns or due to the total energy around 4 ns depending on the component design.

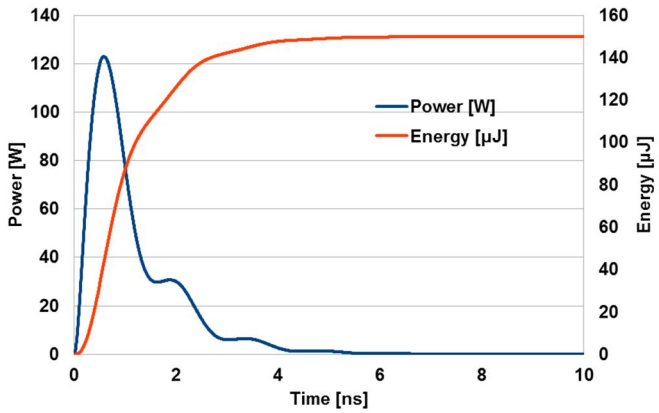

Figure 9. Power and energy curves of an ESD event.

Component failure analysis can show physical damage signatures and reveal what kind of discharge waveforms could be behind the damage signature. Figure 10 shows an ESD failure signature with burnt and melted conductors in a display driver IC due to an excess energy. In this case, the failure required more than 50 μJ energy in the silicon structure to fuse conductors. Figure 11 shows another failure signature where a capacitor has a damaged oxide layer [c]. In this case, the ESD event in an assembly phase was 1.5 ns long having a peak current more than 5 A, an initial discharge source potential was more than 3 kV, a total charge more than 4 nC, and a total energy content more than 6 μJ.

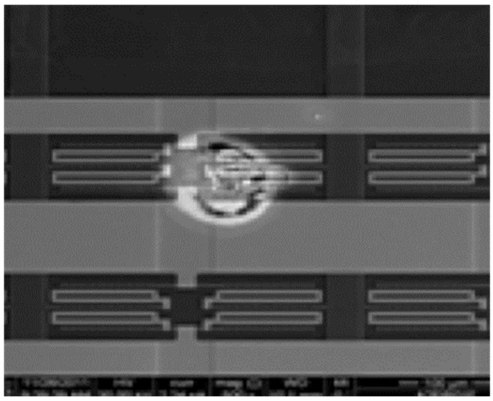

Figure 10. An energy-based failure signature in a display driver IC.

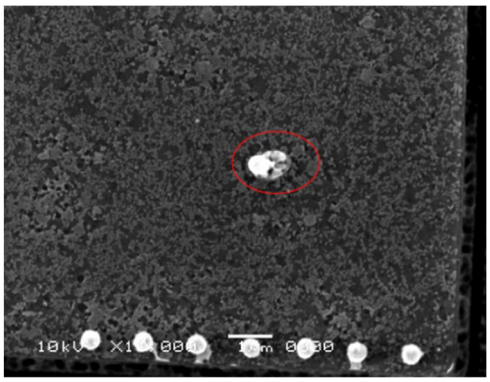

Figure 11. A fused via in the top plate of the capacitor on a silicon oxide due to excess voltage.

ESD type of failure signatures also can origin from system latch up and misapplication events. However, the damage signature can be more extensive than found with ESD events.

4 ESD Protection Techniques with Electronics

4.1 On-chip Protection

Electrical components have on-chip EOS/ESD protection structures integrated into the chip or integrated inside a component package consisting of one or multiple silicon circuits. Several different on-chip protection designs are available such as: serial resistors, parallel capacitors, spark gaps, P/N junction diodes, field devices, RC-triggered power clamps, N-channel MOSFETs, and *silicon controlled rectifiers* (SCR) [1][25][30]–[33]. The basic target of the on-chip protection structures is to limit excess voltage, current, power, and energy of the transient pulse through sensitive areas of the component. This is made mainly by shunting the pulse current waveform into the power supply V_{DD} or ground V_{SS} nodes; thus, the sensitive part of the circuit is no longer along the main current path of the pulse, as shown in Figure 12.

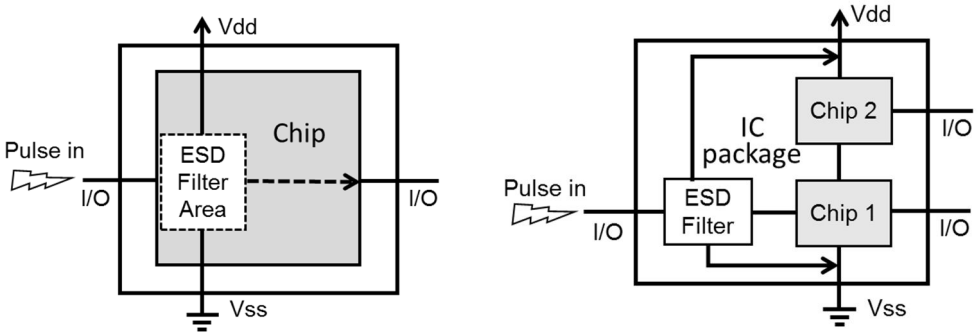

Figure 12. On-chip protection on a chip on the left and inside a multichip IC package on the right side.

On-chip ESD protection structures are typically developed with the aid of a *transmission line pulse* (TLP) method. The TLP was introduced by T. J. Maloney and N. Khurana in 1985, and there are now several different TLP methods available providing controlled shape voltage–current pulses [26]. TLP produces detailed information of a stress event by measuring current–voltage IV curves via and over a DUT, as shown in Figure 13. However, the TPL is not currently used for official component qualification purposes, as it is not part of the qualification standards [27]. TLP can produce different length of pulses between tens of picoseconds up to microseconds. In addition, it can produce varying current rise times starting from about 10 ps with the aid of *very fast TLP* (VFTLP) up to tens of nanoseconds. The IV plot used to develop HBM on-chip protection structures is commonly made with 100 ns long rectangular transient pulses, and the IV point (average current and voltage) is measured in the middle of the pulse, as shown in Figure 13. The 100 ns long pulse has been reported to correlate with the HBM stress levels [28][29]. For CDM design purposes, a VFTLP can use shorter than a few nanosecond long pulses with around the 50 ps rise time. This test method correlates with CDM qualification results but is sensitive to test setup arrangements [30].

A safe operation region of an on-chip protection structure can be presented based on a shaded current–voltage region, as shown in Figure 13 [31]. The lower-voltage boundary *B* is the lowest voltage the IC can still operate, and the upper limit *C* is the maximum allowed transient voltage over the sensitive part of the IC to protect. The on-chip protection turns on when the voltage increases and meets the triggering voltage point *D*. After triggering, the voltage drops to the clamping voltage point *E*, and the current increases toward the *F* based on the dynamic resistance of the protection structure. The limit *A* defines the maximum current the protection structure tolerates without damage when it is a conductive mode, and the point F is often called the I_{t2} failure point. In addition, if the dynamic resistance is too high, the upper-voltage-limit *C* may define the maximum safe operation range for the protection. Therefore, the on-chip protection can have several designed cascaded voltage triggering steps, thus better keeping the IV points inside the boundaries. Finally, the protection structure should turn off when the excess current and voltage have passed the device.

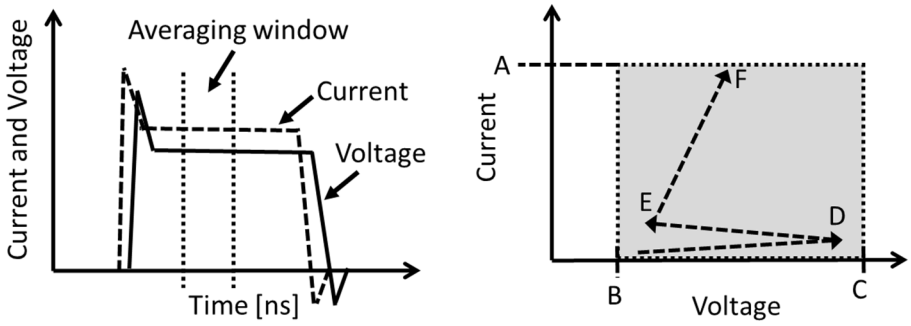

Figure 13. The TLP waveforms on the left; an IV plot on the right.

Several parameters have significant contribution to the efficiency of the on-chip protection and a total IC level ESD robustness [1][21][31]–[34]. Here, the following parameters play a significant role:

- *Triggering voltage* V_{tr} defines the voltage the protection device switch on
- *Dynamic resistance* $R_{on} = (U_b\text{-}U_a) / (I_b\text{-}I_a)$ is the shunting resistance during the conducting phase
- *Turn on speed* t_{tric} explains how long it takes to switch on the protection device
- *Inductance* of the shunting path defines the voltage between the protected I/O and V_{DD} or V_{SS}
- *Capacitance* of the protection device in an off state effects on the high-frequency operation of the I/O line
- *Breakdown* IV point defines the maximum voltage–current rating for the protection structure
- *Leakage current* of the protection device affects the power consumption
- *Durability* of the protection structure define how many stress pulses it survives
- *Clamping voltage* V_{cl} is the set voltage level after the protection structure is switched on
- *Physical size and cost* of the protection structure
- IC is *soldered* or *not soldered* on the PCB, which affects the current distribution
- *On-board protection* components are present or not
- IC is in a *power-on or power-off* state
- I/O has an *external decoupling capacitor* present or not
- *Width and thickness* of the metal wires used on silicon

These operation parameters are contradictory, and it is always a trade-off and case-specific selection, which of the parameters will be emphasized [11]. For example, with high-speed RF I/Os, the input capacitance requirement can prevent use of efficient protection designs, as the maximum allowed parasitic capacitance can be even below 0.1 pF. Ultralow cost components have other challenges with on-chip protection implementation due to the cost penalty; therefore, protection structures can be left out. This is related to the silicon area reservation of the on-chip protection structures, and, without the protection, the chip will be smaller, and more individual components can be produced from a single wafer [35]. The required area for ESD protection on a silicon varies, depending on the used technologies and targeted robustness from a few percent up to tens of percent of the total chip area.

4.2 Human Body Model and Charged Device Model Qualification

An on-chip protection designs are typically qualified with HBM and CDM standards [4]–[7][9]. With a HBM event, there are four different main current paths inside the IC: I/O to I/O, I/O to V_{SS}, I/O to V_{DD}, and V_{SS} to V_{DD} [36]. An HBM discharge source circuit has a 1500 Ω serial resistor and a 100 pF source capacitance, but the inductance can vary [a]. The discharge is given to one pin at the time, and another pin, or a group of pins, is used for the current return path. The standard also defines the current waveform details with the pulse rise time, peak current, decay, and maximum ringing current values for both a short and 500 Ω load [4][b].

CDM sensitivity of IC devices can be tested, for example, according to the standard JS002-2014, and the discharge occurs through one I/O at the time [7]. CDM discharge is fast, having the pulse rise time around 50–100 ps, the peak current varying depending on the DUT, and the total length of the pulse is typically within a few nanoseconds

[b][e][37]. The source capacitance of the ESD event depends on the IC capacitance on the induction plate inside a CDM tester; thus, the stress level depends on the type and size of the component package and the construction of the CDM tester [21][37]–[39][42].

The measured HBM or CDM withstand voltage rating of the IC depends, for example, on the type of I/O connection, used semiconductor technology, type of the on-chip protection, a targeted final product category, data speed of the I/O, and the size of the component package. Therefore, in one IC package, different I/Os may have varying ESD robustness, but the sensitivity of the whole component is reported based on the lowest test voltage all I/Os can pass during a HBM and CDM qualification.

HBM and CDM withstand voltages are independent of each other due to the different ESD failure signatures these two methods produce. The difference of these two events is presented in Figure 14, showing simulated HBM and CDM current pulses with 1 kV discharge potential. The CDM event is over already after a few nanoseconds, whereas HBM current attenuates slowly during hundreds of nanoseconds. The same current waveforms are shown in Figure 15 with the calculated power curves. The peak power of the CDM event is about 10 times higher than with HBM with the same test voltage, and the current rise time is faster. However, the total energy content of the HBM pulse is, in this simulation, 10 times higher than with the CDM due to the fixed 10 times larger 100 pF source capacitance [a]. The generic IC HBM and CDM qualification represents only two failure regions in the Wunsch-Bell-Dwyer graph as the time scale of CDM is close to 1 ns, and HBM events take more than 100 ns, as shown in Figure 15.

Failures generated by CDM can be related to the excess E-field through dielectrics, such as CMOS oxide layers, or to the adiabatic peak power of the pulse. Here, the discharge peak current, which depends on the size and construction of the IC package, is typically the most dominating parameter [21][41][42]. Similar failure mechanisms, as produced by the CDM testing, have been found also in manufacturing fulfilling EPA requirements [a][c][37][43]. On the other side, HBM typically generates failures due to the non-adiabatic heating effect, or the failure occurs due to the excess E-field through dielectrics. HBM is not always such as severe test method, as only part of the pulse energy burns in the DUT. All the current is forced through the DUT, but the 1500 Ω serial resistor limits the voltage over DUT and limits the energy and power stress levels depending on the dynamic resistance of the DUT. For example, if the DUT has 30 Ω resistance during 100 V HBM pulsing, only 2 V (2 %) of the voltage is over the DUT, and only 0.13 W (2 %) of the power heats the device [a].

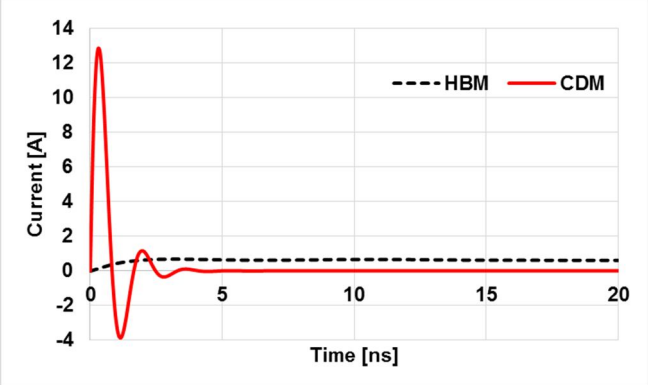

Figure 14. Typical HBM and CDM current waveforms for a large-size IC package with 1 kV initial potential during the first 20 ns.

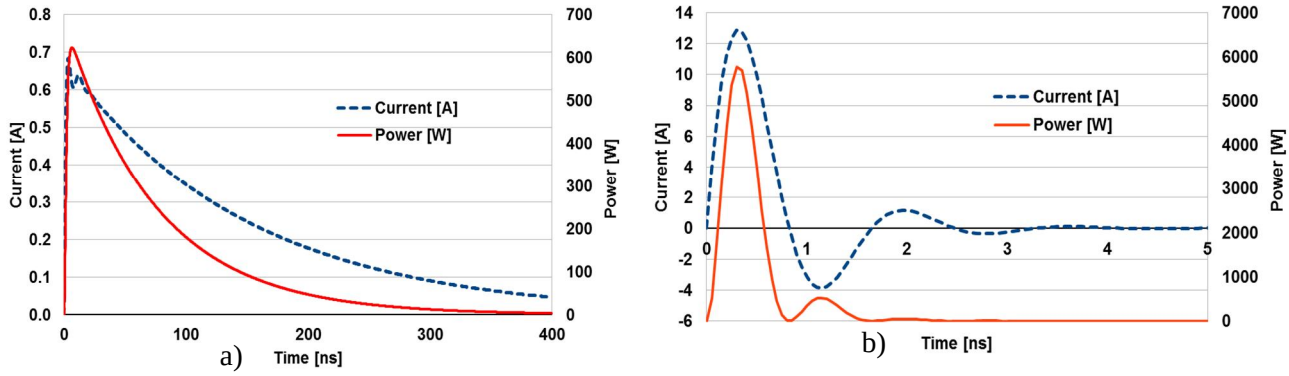

Figure 15. a) HBM current and power; b) CDM current and power.

4.2.1 Correlation of HBM Tests and Real Life Events

The HBM withstand voltage may not necessarily relate to the level of sensitivity of electrical components in a real life situation [a][b]. The initial part of the HBM pulse will vary based on the serial resistance and inductance, and the pulse can create different ESD failures, depending on the turn-on speed of the DUT ESD protection. The real world HBM discharge can have a much faster rise time than given in the standards, and, with over 1 kV discharges, the rise time will vary between 50 ps and a few nanoseconds [v][44][45]. Humidity and the geometry of the physical discharge event also affect the realized HBM current waveform. One example of the real world HBM waveform is presented in Figure 16, using the analyses of Viheriäkoski [v] and Barth [28][44][45]. The figure also has simulated standard HBM waveforms with two different inductance values; L_{min} = 640 nH and L_{max} = 4700 nH, which gives 2 and 10 ns pulse rise times for a short load. However, in a component tester, the rise time is slowed on purpose to meet the standard specification, and the rise time can be more than 10 times slower than the reported real world values [4].

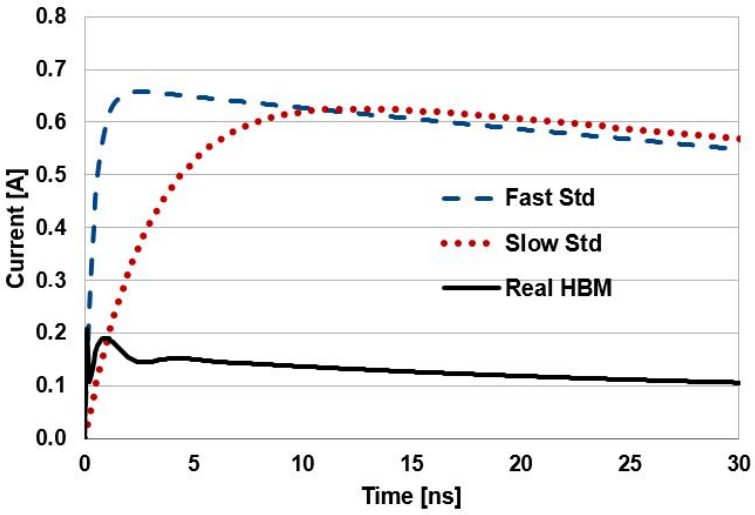

Figure 16. The 1 kV simulated HBM discharge currents with maximum (tr=10 ns) and minimum (tr=2 ns) rise time based on the ANSI/ESDA/JEDEC JS-001-2011 standard. A measured 1 kV real life HBM discharge for comparison.

The resistance of the real HBM event depends on the discharge voltage, and only with over 2000 V potentials is the resistance close to the standard 1500 Ω. Here one of the varying parameters is the skin resistivity. The results were presented in a reference paper [v]. The HBM tester setup and the real world discharge parameters are compared in Figure 17. Below 500 V, the human body resistance is significantly higher than that of the standard values [v][46]. With 100 V level the real world discharge has a peak current of about 0.6 mA, which is about 100 times lower than a typical HBM stress with 100 V in a tester.

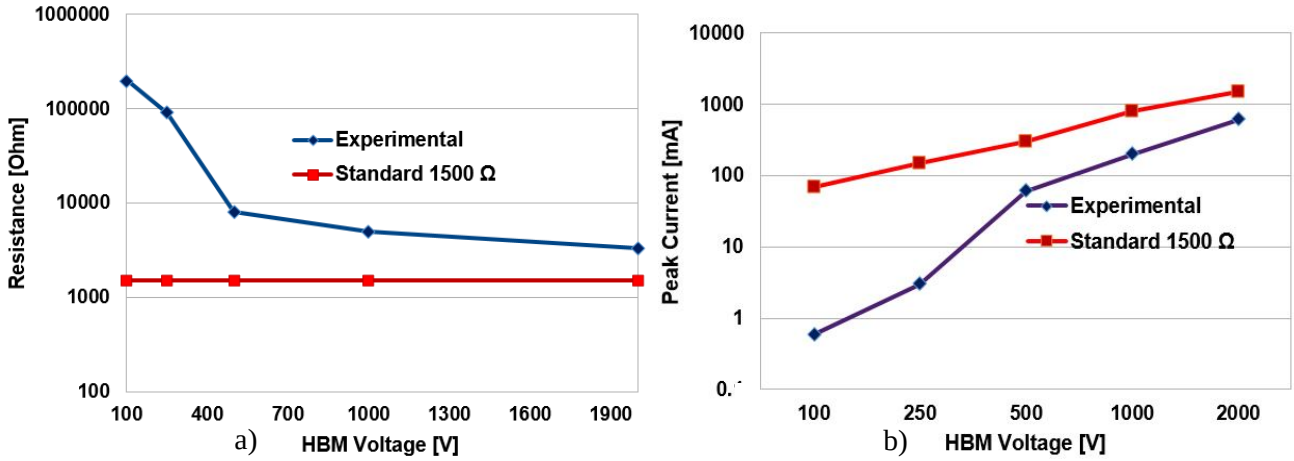

Figure 17. Left a) Resistance of the HBM in a standard test set-up and in a real world discharge event.

Right b) Peak currents in the standard test setup and in a real world discharge event.

Component ESD robustness against HBM discharge is reported by using the maximum discharge voltage the DUT survived [a][4]. Sometimes, the most sensitive pin combination data is available, but this data is not visible on most component data sheets. In addition, not all pin combinations are tested in order to decrease testing time and prevent excessive ESD stress [1][4]. What is also missing from the data sheets is the exact failure current, the rise time of the pulse, and the failure type with its reported voltage level. The maximum safe discharge charge Q (nC) can be calculated based on the known voltage and 100 pF source capacitance, but that charge can be irrelevant without the exact current and time (I_{t2}) failure information [47][48]. The HBM current distribution along I/Os can also have major differences in a qualification phase and after the IC is soldered on a PCB. Table 1 has more detailed information of typical HBM discharge parameters in a qualification phase.

Table 1. Short-circuit HBM discharge parameters with *RLC* values of 1500 Ω, 1000 nH, and 100 pF.

Voltage	Rise Time	Peak Current	Charge	Energy	Peak power	Max dI/dt
[V]	[ns]	[mA]	[nC]	[µJ]	[W]	[A/ns]
50	2.8	33	5	0,13	1,6	0.05
100	2.8	65	10	0,5	6,4	0.1
200	2.8	130	20	2	26	0.2
400	2.8	260	40	8	103	0.4
800	2.8	520	80	32	410	0.8

In summary, discharge events in a component HBM qualification test and in the real world have major differences; therefore, it is challenging to use HBM withstand voltage information to estimate ESD risks in electronics assembly processes.

4.2.2 CDM Withstand Voltage Correlation with Real Life CDM Events

The reported CDM withstand voltage alone is a pretty hazy value to use to estimate ESD risks in a real process [a][b][31][38]–[43]. The voltage is the maximum level IC devices that survived in a tester, but the reported voltage is not the same voltage level as that used in a CDM tester during the stress test. The voltage in a tester is adjusted based on the CDM discharge peak current target during the tester calibration phase. Different CDM standards also stress the device at different current levels with the same reported voltage. Here, one source of uncertainty comes from the 1 Ω disk resistor current sensor itself where the 3 dB cut-off frequency response can attenuate the peak current value above 1 GHz [39]. A resistance of the air spark is time dependent and is typically around 25 Ω, but it has also a large variation; thus, affecting the stress level as shown in Figure 18. The varying air spark resistance has been reported to be one of the main sources of uncertainty with CDM testing. The IC device itself also causes a lot of variation in the realized CDM stress level, as the construction and capacitance of the component in a tester are not taken into account when the withstand voltage is reported.

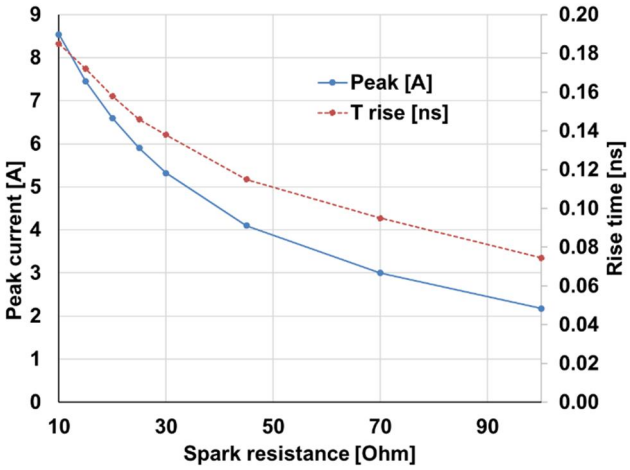

Figure 18. A calculated CDM peak current and pulse rise time with varying spark resistances.

There are alternative CDM test methods available, such as *capacitively coupled TLP* (CC-TLP), *wafer-level CDM* (WCDM) and CDM2 methods, which have better repeatability than the FICDM method [21]. With CC-TLP and CDM2 methods, the discharges are made with a direct contact on DUT; thus, there is no variation from the air gap. In addition, these methods can produce similar failures, as with the FICDM method even the shape of the discharge current pulse is not exactly the same. However, these methods are not yet commonly used for component qualification, as the methods are not part of the CDM test method standards.

Typical CDM discharge parameters in a FICDM testing, which are based on the selected RLC parameters, are presented in White Paper 2 [31] and calculated also in Table 2 with 35 Ω serial resistance.

Table 2. Calculated CDM discharge parameters with the following RLC values: 35 Ω, 5 nH, and 2 pF.

Voltage	Rise Time	Peak Current	Charge	Energy	Peak power	Max dI/dt
[V]	[ps]	[A]	[nC]	[µJ]	[W]	[A/ns]
50	100	0.64	0.1	3	14	10
100	100	1.27	0.2	10	57	20
200	100	2.5	0.4	40	225	40
400	100	5	0.8	160	900	80
800	100	10	1.6	640	3600	160

With large-size ICs, the dynamic capacitance between the component and the field plate of the CDM tester can be larger than the capacitance between the field plate and the ground plane. Therefore, the peak discharge current will not linearly increase with the stress voltage, and in a real world discharge case the dynamic capacitance can be even larger, thus, the CDM peak current is higher than in a tester with the same potential level [38][39].

As a summary, the CDM tester environment represents a typical worst-case discharge scenario, one not easily found in real life scenarios [49][50]. From this point of view, it is thus possible to estimate that an IC device should survive a discharge at least with the reported CDM voltage in EPA. However, in real life this relationship has uncertainties and can lead to underestimation and overkill with ESD protection methods in EPA [c][viii][31][37][41][43][49]–[52].

4.3 System Level Protection Designs

Electronic products have basically four levels of EMC/ESD protection. The first level is a system enclosure, which is typically made of a dielectric plastic or conductive metal. The second level is an air gap among the enclosure, PCBs, and parts inside. The third level is build-up with a ground layers and on-board protection components on the PCB, and the last level is the on-chip protection inside ICs [53].

A basic design for the total system-level protection and designed main discharge current paths are shown in Figure 19. The enclosure is typically the main protection method and can prevent most of the destructive ESD events. Therefore, a well build enclosure requires no more ESD protection for electronics inside. A conductive solid metallic enclosure is typically the most robust against both EMC and ESD but is more expensive than a plastic, and most enclosures use mixed materials depending on the functionality and visual requirements. However, in electronics assembly and testing phases, enclosures are not always present, and the enclosures have seams, gaps, connectors, and other holes, which can leak discharge current or RF noise inside.

A plastic enclosure with more than 0.1 mm thickness can already protect the system from conductive discharges, but when an ESD spark hits the enclosure surface, there can still be a high-frequency current flow due to a capacitive coupling and secondary sparks between the ESD source and electronics inside [54][55]. This is related to a low electromagnetic field shielding properties of dielectric plastic materials. More challenge comes from secondary discharges and seams and holes on a plastic enclosure, and these may require ground rings or other conductive layers to capture the ESD spark and to protect the system [53][54][56].

As the second level, the protection can be accomplished with a large enough air gap, but this depends on the type of product and cannot be used as well, for example, with small-size electronic systems. A generic rule is to predict that the electrostatic field breakdown strength of an air is approximately 3 kV/mm, and, thereby, a 1 mm air gap can isolate 3 kV air discharges. However, the gap needs to be from a few millimeters up to about 15 mm deep to prevent spark jumping when the system is qualified with 15 kV air discharges according to the IEC61000-4-2. Discharge channels can also travel in narrow enclosure gaps and along the surface of a dielectric material further than the air breakdown field strength predicts [53].

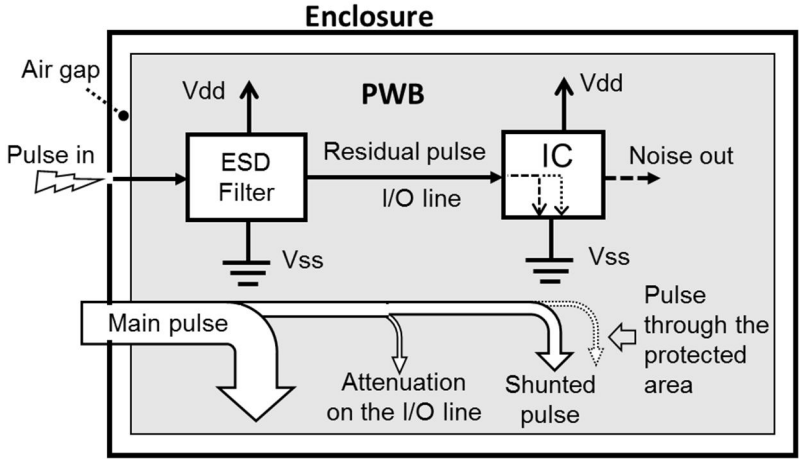

Figure 19. ESD protection with electronic products.

At the third level, on-board EMC/ESD filters and discrete components are used to protect ICs, reduce EMC/ESD coupling issues, and to maintain signal integrity. Figure 20 shows 10 generic example on-board protection circuits used with product internal and external I/O connections [32]. Parallel capacitors in the figure and the exact values of the capacitors are optional but commonly used to reduce EMC noise coupling and emissions from RF systems. The protection designs *O, B, E,* and *H* can be used to filter system level IEC61000-4-2 pulses depending on the selected components. The designs *E* is for high voltage applications and for systems with high RF signal coupling. Designs *A, C, D,* and *F* have limited protection efficiency against ESD but can still attenuate the stress level. The design *G* with a spark gap has a low input capacitance and can be used to protect high-speed RF I/O lines. However, spark gaps have typically significant residual stress levels due to the over 200 V triggering voltage and cannot typically protect sensitive RF I/Os from direct IEC61000-4-2 discharges. The component *X* is a common mode choke used to protect cable connections from external EMC/ESD noise. There also are a high number of different application-specific integrated parts (ASIP) components available for EMC and ESD filtering purposes [32][53]. An ASIP may include active transistors, diodes, coils, and discrete components in a single IC package. These components are commonly used to protect, for example, connector I/Os, which are accessible in a final

system. In ultralow electronics, ASIPs are less used protection technology due to relatively high cost in comparison with protection designs, as shown in Figure 20.

The on-board and on-chip protections may not be designed to tolerate other than residual parts of IEC61000-4-2 pulses or standardized HBM and CDM discharges. On-board filters also are added in a PCB layout typically only for specific I/O lines going to be stressed in a final system and will be assembled only if required to get the system through EMC immunity and emission qualification tests. During system designed optimization rounds, these filters may be left out to decrease material costs. On-board protection components are neither typically available in I/O lines transferring data between separate subassemblies if those are not going to be stressed in a final system.

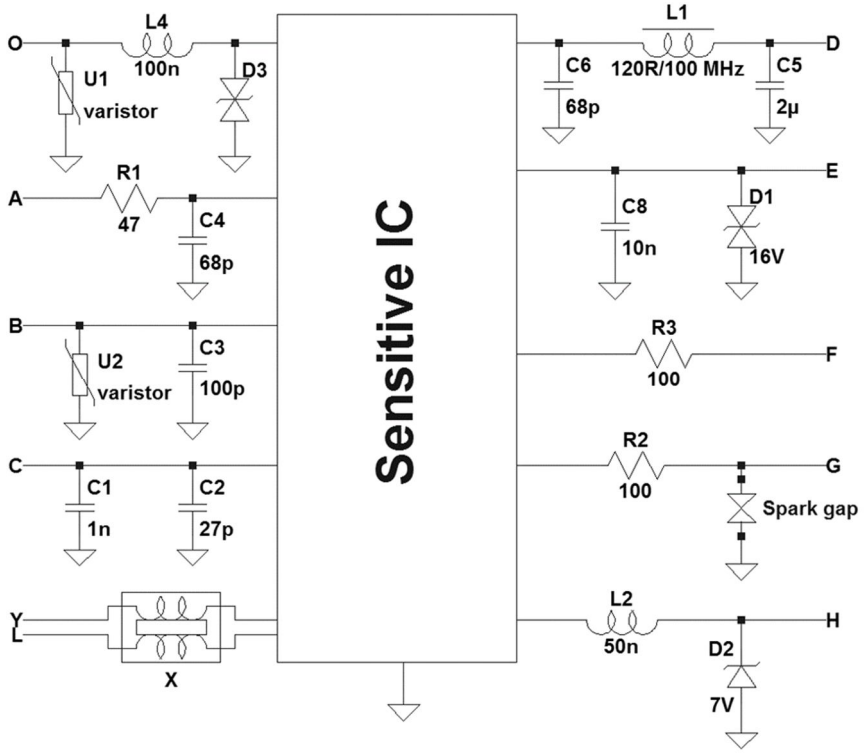

Figure 20. Generic on-board EMC/ESD protection circuits, which are used to protect sensitive I/Os.

During electronic assembly phases, system-level EMC/ESD protection designs are typically not fully functional. When the enclosure is not in place, or is even partially missing, the PCB and electrical connections are accessible and may be contacted with assembly tools, tester pogo pins, and with additional installed components. Thereby, the only ESD protection available is from on-board protection designs and component internal on-chip protection structures. However, on-board protection is typically available only in specific I/O lines and traces, and those may not be the same as contacted during the assembly. In addition, in the assembly, single ICs and modules are placed on the PCB, and there can be a direct contact between the PCB and IC without any external protection. In summary, ESD stress events in electronics assembly phase may vary, and ESD risks are product and process specific and require stepwise analysis [a][c][d][36][37][43][47] [55][56][59][60].

4.4 System-Level ESD Qualification

In the European Union, a type approval of a final electronic system includes an EMC/ESD immunity test, according to the IEC61000-4-2 standard [16]. This test method is commonly used also all over the world to qualify electronic equipment. In addition, when a specific I/O line of an electronic system can be accessed by the end user, or the IC will be used in a harsh environment, the required IC or subassembly level qualification waveform can be set based on the IEC 61000-4-2 specification, even this is not the official way to operate [1][4][7][16][31][32][61][62][63]. This is supported by the known challenges to use the IEC 61000-4-2 standard to test ICs [64]–[68]. This standard is targeted only to test complete electrical systems, and there can be significant variation with the stress levels on IC level, depending on how the test setup has been arranged. In addition, the

discharge waveform has a relative large accepted variation with ±15 % peak current and ±30 % current at 30 and 60 ns points during a calibration phase [16].

During the qualification, the *equipment under test* (EUT) is placed on a wooden test bench or on a flooring with a horizontal ground reference plane and a 0.5 mm thick dielectric layer on top of the ground. The EUT is a complete final system; it can be electrically floating, or it can be grounded via power source or data connection cables. Conductive areas of the EUT are tested with negative and positive contact discharges typically up to 2–8 kV, and dielectric surfaces are tested with air discharges typically up to 8–15 kV. Higher stress levels up to 30 kV can be used, for example, with automotive, military, and aviation electronics [60][61]. For example, a *local interconnect network* (LIN) interface needs to withstand direct system-level ESD currents and radiated electromagnetic pulses up to 15–30 kV [61]. The DUT has to survive IEC 61000-4-2 tests without hard failures and without disturbances depending on the selected performance criteria.

The IEC 61000-4-2 qualification produces radiated EMI and high conductive current ESD pulses [16] [66][69][70]. The source of an IEC 61000-4-2 current waveform can be simulated by using equations (5)–(7) with two parallel RLC networks with the following example parameters: R_1≈370 Ω, L_1≈3800 nH, C_1≈140 pF, and R_2≈180 Ω, L_2≈180 nH, C_2≈10 pF [16][63][71][72]. The first RLC circuit produces an overdamped current pulse with high energy content, and the second circuit forms the fast initial part of the pulse, as shown in Figure 21. The fast part of the pulse represents a discharge from a small metallic hand tool, and the following part simulates the discharge from rest of the human body through the tool. However, the exact RLC parameters and the waveform vary between different pulse generators; thus, to more accurately simulate the real life waveforms requires us to include radiated electromagnetic pulses in the simulation method. This requires us to use 3D simulation tools and accurate modelling of the discharge environment [69][73][74].

System qualification tests produce pass/fail data, which are not easy to transfer for ESD risk assessments in an electronics manufacturing environment, as the tests are made for complete systems above a ground reference plate. In addition, individual subassemblies may not be tested with IEC pulses; in that case, the test result would be a pass/fail type with limited details of the real stress level the subassembly will see. For example, it is typically not known how much current or voltage single I/Os will see on the PCB during the system qualification. In addition, connectors or test pads inside the system enclosure are not tested during the system-level qualification.

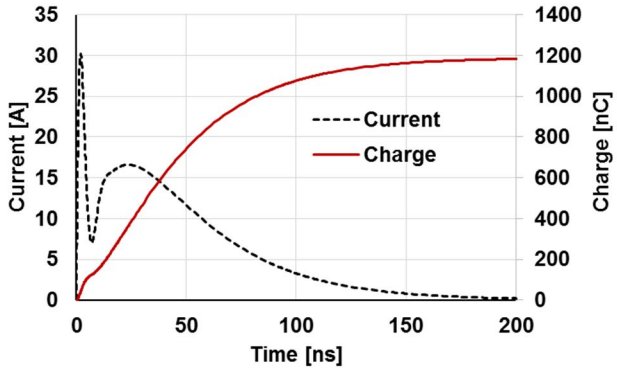

Figure 21. IEC 61000-4-2 current waveform with 8 kV with two-ohm calibration load.

4.5 Subassembly-Level ESD Sensitivity

There is not an agreed-upon method available on how to test subassembly-level ESD immunity. The IEC 61000-4-2 standard test method is valid only for completed systems, but a subassembly, such as a PCB without an enclosure, may not be designed to tolerate direct IEC stress waveforms. It would also be too expensive to design and build subassemblies to survive against system IEC qualification test levels. However, there have been additional test methods developed, such as a *charge board event* (CBE), *cable discharge event* (CDE), and modified CDM testers that simulate real world ESD scenarios [a][f][ix][31][75]–[80]. A typical need for such a test is during product handling and assembly, where it may be required to know more in detail what level of ESD

pulses can disturb or damage products. These discharge events include cases where a charged component, cable, or product itself is the source of discharge. With the CBE, CDM, and CDE, the discharge current waveform is device dependent and simulates a discharge scenario where the waveform is a step response of the circuit when the charged object is grounded. The main difference between the CBE/CDE and CDM is that CDM has fixed discharge setup parameters, whereas CBE/CDE can have all parameters as variable.

4.5.1 Charged Board Event Test Method

CBE discharges can be made by charging a DUT to a selected potential and then discharging it with a ground contact. The resulting discharge current is typically similar to Figure 7 waveforms if the contact is made with a grounded wire. However, there can also be discharges between non-grounded subassemblies where the potential level equalizes, and the same total quasi-static charge remains in the objects after the event.

To measure the discharge current requires us to add a current probe along the discharge path. However, this changes the discharge scenario due to an additional discharge path inductance and resistance. In addition, a capacitive coupling between the non-grounded objects changes the quasi-static potentials when the objects approach each other. Another way to conduct CBE tests with subassemblies is presented in Figure 22 and Figure 23 [31]. In this case, the DUT is charged with induction in a similar way as is used in a field-induced CDM tester. The discharge can be made with a ground wire, but it is possible to discharge the DUT also with another conductive subassembly and still calculate most of the discharge parameters by monitoring the quasi-static potential level of the induction plate.

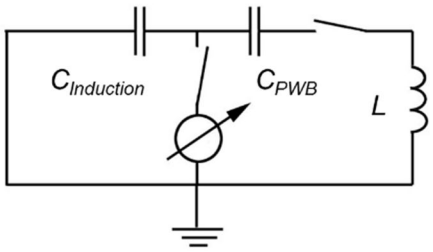

Figure 22. CBE equivalent circuit.

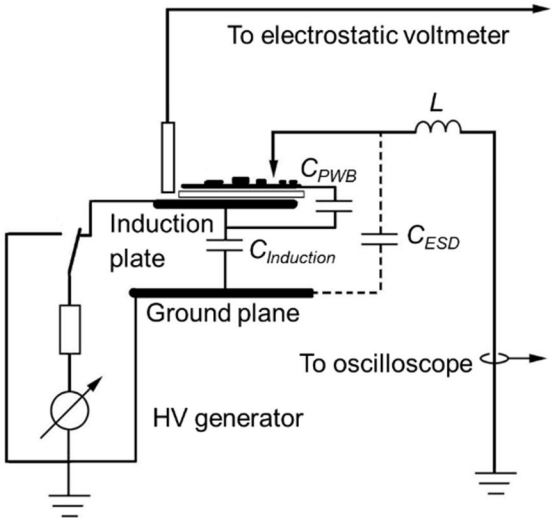

Figure 23. CBE test setup.

Figure 23 shows that an electrostatic voltmeter measures the potential of the induction plate. In addition, the capacitance of the induction plate can be measured with a capacitance meter or by using a voltmeter, charge meter, and equation (1). By using the initial and residual voltage data and $C_{Induction}$ information, the discharge capacitance C_{ESD} and the capacitance of the printed wiring board C_{PWB}, the total energy of the discharge, and the total movable

charge can be calculated with equations (1), (2), (8)–(11). A resonance frequency and the inductance of the discharge circuit can be calculated only if a current probe is used along to the discharge path.

$$C_{ESD} = \frac{C_{Induction} \cdot V_{Initial} - C_{Induction} \cdot V_{Residual}}{V_{Initial}} \qquad (8)$$

$$C_{ESD} = \left(\frac{C_{Induction} \cdot C_{PWB}}{C_{Induction} + C_{PWB}} \right) \qquad (9)$$

$$C_{PWB} = \left(\frac{C_{Induction} \cdot C_{ESD}}{C_{Induction} - C_{ESD}} \right) \qquad (10)$$

$$L = \frac{\left(\frac{1}{2 \pi f_0} \right)^2}{C_{ESD}} \qquad (11)$$

With equations (8)–(11), $V_{Initial}$ is the quasi-static potential of the induction plate before ESD, $V_{Residual}$ is the potential of the induction plate after ESD, C_{ESD} is the capacitance of the discharge circuit, C_{PWB} is the capacitance between the circuit board and induction plate, $C_{Induction}$ is the capacitance between the induction plate and the ground plane, Q_{Mobile} is the transferable charge of the discharge circuit, E_{ESD} is the calculated energy of the discharge based on equation (2), and L is the calculated inductance from a resonate frequency f_0, when applicable.

Simulations by using equations (5)–(7) can be used to verify and fine-tune CBE stress levels. The CBE waveforms can be simulated quite reliably also by 3D simulators and SPICE tools. The biggest challenge is to accurately model all of the parameters. CST Microwave studio with finite integration simulation techniques (FIT) in a time domain and SPICE simulation methods are presented in several papers [f][iii][iv][ix][80]–[82].

A subassembly can have a high number of conductive leads, test pads, and other electrical connections that can be contacted during handling. However, typically only a few of these contact points will be touched during assembly, testing and programming. Therefore, it is typically only necessarily to stress a few contact points based on product and process specific ESD risk analysis. More detailed description of the CBE test procedure is given in Chapter 6.

4.5.2 Field Collapse Event Test Method

There can also be subassembly discharge scenarios where an ESDS is grounded and will be influenced by a fast-changing electrostatic field. In addition, the subassembly or a system can be powered, or there are several cables connected into the system to monitor system functionality. In that case, CBE discharges cannot be made, as the system cannot be charged with induction or by using contact charging methods.

To carry out CBE type of testing for grounded devices, a *field collapse event* (FCE) test method can be used [f][ix]. FCE bases on a fast-changing electric field, which drives current into a DUT by induction. CDM, FCE, and CBE are based on the same initial setup, where the DUT is placed on top of a known dielectric layer, which is on a conductive induction plate with a known capacitance. The induction plate is electrically floating and is charged up to a selected voltage, which creates an electrostatic field around the plate. This field is used to charge the DUT. With the FCE method, the discharge event is initiated by grounding the charged induction plate. The DUT grounding point, or points, also are the DUT stress points similar to CBE or CDM, but these two methods have always only one grounding point: the ground contact point.

The main benefits of the FCE method over CDM and CBE are that the DUT is continuously grounded during the discharge, and an air spark is not along the DUT ground path. In addition, DUT can be in a power-on state, and it is possible to measure DUT parameters with high impedance current and voltage probes during ESD tests. Discharge waveforms can also be adjusted by varying the test setup dimensions and by varying the discharge path resistance, inductance, and capacitance (RLC) parameters.

A simplified FCE test setup is presented in Figure 25, and an equivalent circuit for the setup is shown in Figure 24. The current I_{Tot} flowing through the induction plate discharge wire is a sum of two main currents: I_1 and I_2. I_{Tot} is a complex waveform, as there are three capacitances, two parasitic inductances, and two dynamic resistances affecting on the realized current. The DUT discharge current I_1 is the most interesting parameter to monitor, and it can be measured with a current transformer along a ground wire shown in Figure 25. The total initial capacitance of the test setup is $C_{Tot} = C_{Ind} + C_{DUT}$. However, DUT has only the capacitance C_{DUT} left when the discharge is initiated by grounding the induction plate with a charge stored in the C_{Ind}. Thereby, the total discharge energy of the event can be adjusted by selecting the potential level, size of the induction plate, and the dielectric material between the DUT and the induction plate.

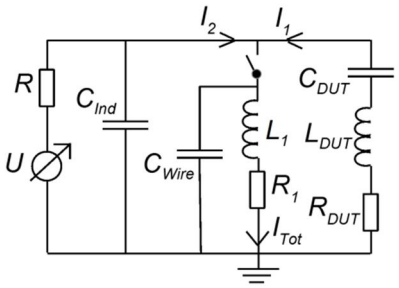

Figure 24. FCE equivalent circuit.

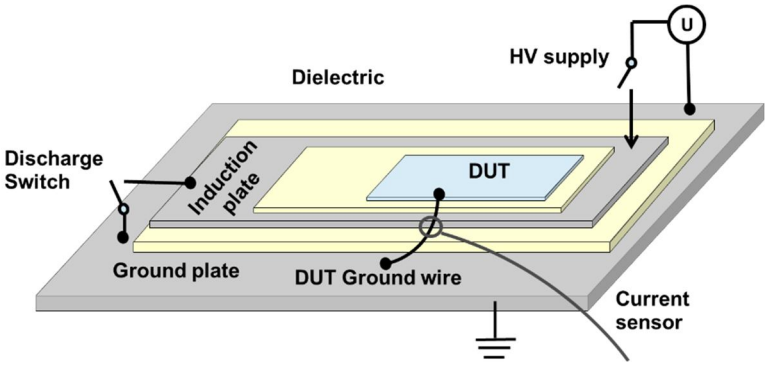

Figure 25. FCE test setup.

FCE discharge waveforms are more complex to model with mathematical equations than CDM or CBE events, as there are several nonlinear varying components in serial and parallel connections. However, FCE discharge scenarios can be simulated with a SPICE software tool by using an equivalent circuit, as shown in Figure 24. In that case, the switch is replaced with a voltage source that gives a step voltage function. Simulated and measured discharge current waveforms can show good correlation, as shown in Figure 26 [f].

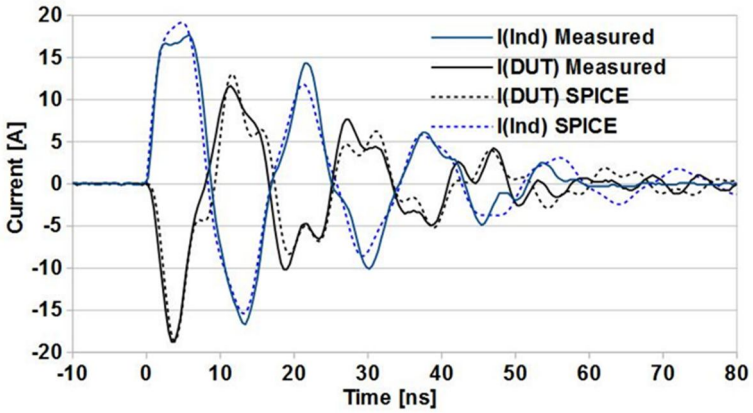

Figure 26. FCE measurement and SPICE simulation results.

The source capacitance of CBE is a serial capacitance of C_{Ind} and C_{DUT}. In FCE, the capacitances C_{Ind} and C_{DUT} are in parallel; therefore, FCE has a higher DUT stress level with the same initial charging voltage. However, if the DUT is grounded via several wires in a FCE test setup, the ESD stress is shared between the connections. The exact stress level depends on the PCB circuit design and the type of connections used to ground each DUT stress point.

4.5.3 Charged Cable Discharge Event Tests

Charged isolated cables can produce similar discharge current waveforms as obtained with TLP testers and can be approximated by a square pulse of 1.5–3.0 A for each 1 kV charging voltage [27][81][83][84]. However, with very long cables measured in tens of meters, the pulse shape is no longer rectangular but more like a decaying curve or a curve with multiple reflections [84][85]. In addition, if the other end of the cable is connected to non-grounded equipment, the waveform is a combination of CDE and CBE pulses [xi][81]. CDE has typically a high initial current peak, which can produce similar failures as found with CDM, IEC 61400-4-2, and fast CBE discharges. In addition, the total energy of the CDE depends on the length of the cable; thereby, with the same initial potential level, long charged cables can produce more energy-based failures than short cables with less stored charge [85].

Due to the shape of the CDE waveform, TLP testing can be used to simulate cable discharges. In addition, CDE testing can be done by charging an isolated cable and discharging it via a short wire with a current probe onto the selected pin in a DUT connector. This is a similar test method and setup as used with CBE testing.

4.6 A Comparison of Different Discharge Events

Discharge parameters for the five scenarios are presented in Table 3 with a 100 V initial charge level. Here the main purpose of the Table 3 is to show differences between the ESD events when the initial charge voltage is kept constant. The parameters can vary significantly with higher initial charge levels.

CDM can damage electronics due to a high peak current, current rise time, and power levels, even when the total transferred energy content is low. *Human metal model* (HMM) events simulating IEC 61000-4-2 discharges have even higher charge transfer and peak current levels, whereas HBM events are the weakest [63]. CBE and CDE can have generally significantly higher stress levels except with a current rise time, which is the fastest with CDM events. CDM/CBE/CDE are also realistic ESD scenarios in EPA, and, due to high stress levels, these can easily damage electronics. In addition, real life HBM and CDM events have highly varying rise times, peak currents, source capacitance, power, and energy content. Similarly, CBE/CDE/HMM events will vary depending on the environment, the voltage stress level, and on the electrical parameters of the objects taking part in the ESD event.

Applying Table 3, any safe potential limit is difficult to give for any of these discharge scenarios, as the product itself and the close environment defines the stress level; thus, several discharge parameters are required to define the severity of an ESD event fully. An exact risk estimation would require product sensitivity tests with the real world discharge waveforms found in the handling process and should be undertaken in a controlled laboratory environment. At any rate, product sensitivity analysis can still be carried out and used to assess real world process ESD risks, as presented in several publications [c][d][xii][12][43][47][50][56][59][75]–[86].

Table 3. Example discharge parameters with a 100 V initial charge level.

100 V	Rise Time	Peak Current	Charge	Energy	Peak power	Max dI/dt
	[ns]	[A]	[nC]	[µJ]	[W]	[A/ns]
HBM[1]	2.8	0.065	10	0,5	6,4	0.1
CDM[2]	<0.1	1.27	0.2	0.01	57	<20
HMM[3]	0.1 - 3	<0.5	15	0.5	<20	<10
CBE[4]	0.1 - 3	<10	<10	<1.5	<500	<15
CDE[4]	0.1 - 3	<10	<10	<1.5	<500	<15

Note: [1)] from Table 1, [2)] from Table 2, [3)] based on IEC 61000-4-2 test setup simulations, [4)] with <40 nH serial inductance

5 ESD Risks in Electronics Assembly

5.1 Electrostatic Protected Area

A noncontrolled environment can produce unpredictable ESD risks in electronics manufacturing and cause high-yield losses [2][viii][xii]. Therefore, it is necessarily to protect electronics against ESD during handling and manufacturing, even if there are on-chip, on-board, and system-level protection designs in place. This is accomplished with the aid of an electrostatic protected area and an ESD control program plan, which defines how to design, establish, implement, and maintain the program with administrative and technical requirements [14][15].

The control plan should include three main sections: a training plan, a compliance verification plan, and technical requirements. In addition, there can be detailed information, for example, about grounding methods, packages, and markings used in EPA. A type and size of an EPA can vary largely from a single person working bench to a 200,000m^2 size large manufacturing area with more than 10,000 persons and thousands of process equipment.

The main protection methods in EPA are:

- All conductors in the environment, including personnel, shall be bonded or electrically connected and attached to a known ground or contrived ground
- Avoid a discharge from any charged, conductive object
- Avoid a discharge from any charged ESD sensitive device
- Avoid a discharge from any conductive object with induced voltages
- Use ESD protective packaging outside EPA when necessarily
- Train the personnel to understand the control principles
- Carry out compliance verification tasks to monitor the EPA
- Follow technical requirements set for groundings and material properties
- Neutralize charged isolated conductors before contacting ESDS
- Mark clearly the boundaries of EPAs

In principle, these methods are clear to follow, but the ANSI/ESD and IEC standards and complementing technical reports do not define exact methods for the EPA establishment and control; instead, the program and EPA need to be tailored based on the electrical products and type of the facility. The current standards focus mostly on personnel groundings, EPA item groundings, efficiency of the ionization, and ESD safe packaging materials. These items are similar in most EPA, and therefore, easier to define in standard documents. In addition, these covers mostly the first two layers *EPA* and *equipment* presented in Figure 27.

Standard documents do not have detailed information, for example, on how to estimate ESD risks related to the handling processes or how to measure product part or cable charging and discharging during compliance verification [a][b]. These are largely varying, depending on the used processes and products, and are mainly covered by the two top layers *equipment* and *products* of the Figure 27. A detailed ESD control program covering all the three layers can have tens of pages' technical rules, compliance verification methods, and guidelines the local ESD responsible needs to maintain and follow.

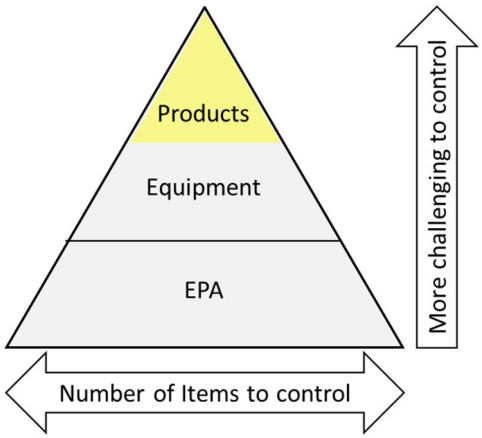

Figure 27. Three layers of an ESD control program.

The three layers of the Figure 27 also depend on each other, as it would be challenging to control ESD risks with equipment or ESD risks with product part handling, if the close environment is not under control. Here, the EPA ground network, and reliable ground connections forms a base stone for the ESD control.

Figure 28 presents an example grounding plan for the equipment grounding and the methods to ground nonelectrical fixed installations via additional EPA ground. These two ground networks should be bonded together only in a facility main earth bar. On top of these items, there can be working surfaces, floorings, shoes, gloves, jigs, adapters, trays, ionizers, tools, grippers, and many other materials in EPA that need to fulfill the control program technical ground resistance requirements. Unfortunately, there can be cost, durability, process, material qualification methods, and logistic related limitations that forces us to use noncompliant materials in EPA breaking the electrical ground path [vi][87][88]. For example, non-ESDS subassemblies are typically stored in dielectric packages, which are cheaper than electrostatic dissipative packages; thus, these parts may receive electrostatic charges via triboelectrification and induce potentials or discharge on ESDS items when assembled together. Here, the ground path cannot remove charges, and additional preventive actions may be needed. A common active protection method is to add ionizers to neutralize charged objects, but ionizers can be too slow to neutralize objects in fast assembly processes. In addition, ionizers add ESD related investments and require periodic maintenance.

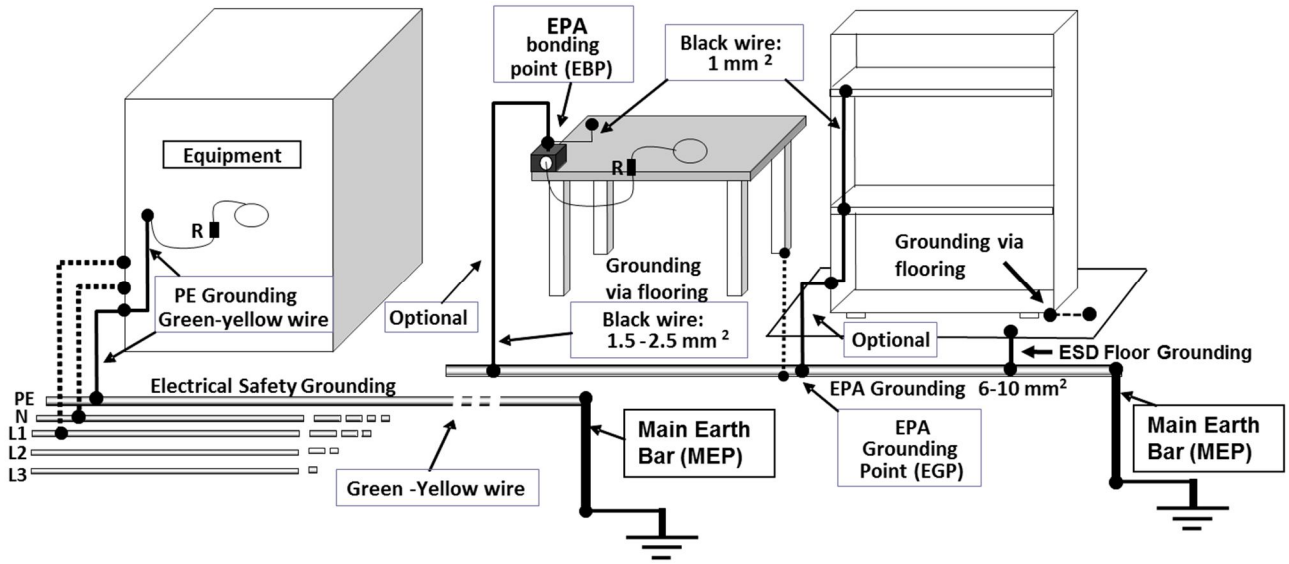

Figure 28. A basic EPA grounding schematic.

The ground network presented in Figure 28 has typically several deviations in a real world EPA. Anodized aluminum is commonly used to construct process equipment. However, anodized surfaces easily break electrical

connections. Working tables can be made of composite or wooden materials without electrical conductivity. Therefore, a solid EPA ground network is challenging to implement and keep consistent.

ESD SP10.1 and ESDA Technical Report 14-02 give some guidance for the ESD protection design and testing of *automated handling equipment* (AHE) [89]. The following principles of ESD prevention are equally important in assembly processes [e][i][ii][31][47][59].

- All conductors are equipotential bonded (and preferably grounded)
- All non-essential insulating materials are excluded
- Materials and equipment designed for use in the equipment have carefully controlled charge generation and dissipation properties
- Use dissipative material to contact ESDS
- Where insulating materials are necessarily present, the charge on these is minimized by measures such as ion neutralization.

Figure 29 and Figure 30 show example drawings used to construct ESD safe AHE designs [ii]. Here, the black color indicates a conductor with less than 5 Ω resistance to the ground, and the solid gray color is a dissipative material with 10^4–10^9 Ω resistance to the ground. Movable metal objects have to have less than 1 MΩ to the ground. Basically, the same rules apply to any automated equipment handling ESDS.

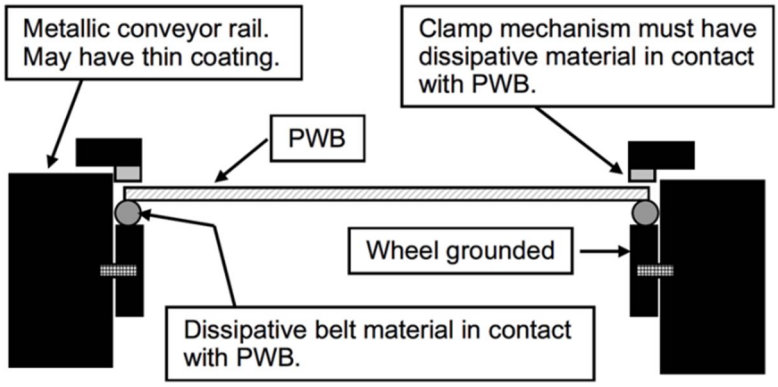

Figure 29. An ESD safe conveyor design.

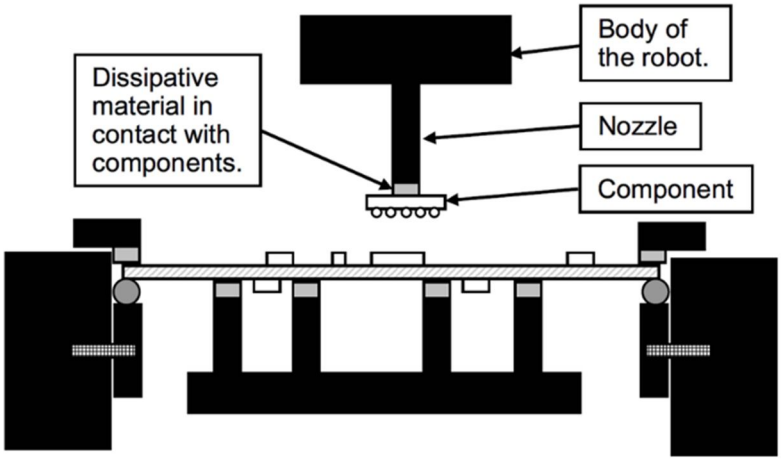

Figure 30. An ESD safe component assembly station with a PCB clamp, center support, and placement head.

Electronic test equipment and products can be sensitive to transient electromagnetic noise and ground-voltage bouncing in EPA [90]. For example, switching on and off a reflow oven can disturb electrical systems connected to the same power or ground network. These disturbance events can be difficult to detect when those occur only a few times in a day or hour but can still cause major yield losses in EPA [d].

5.2 Observed Electrical Failures and Disturbance Cases in Electrostatic Protected Areas

Electrostatic protected areas can effectively prevent ESD failures from charged operators, work benches, and tools. However, electrical disturbances and ESD events from other sources can still exist in well-built EPAs. These failure cases were analyzed in the reference publications [c][d], and similar cases have been reported in other references [12][31][36][43][47][58][59][77][86][90].

The main purpose was to analyze the type and reason of the observed failures and produce information to further improve ESD control programs and electromagnetic compatibility related risk prevention.

The failure cases were collected from electronics assembly environment in different companies between 2005 and 2015 [d]. All the cases occurred in EPAs mostly meeting both ANSI and IEC standard requirements and the analysis based on 42 individual failures. The data were collected from manufacturing sites located in Europe, Asia, and South America and included both *original equipment manufacturer* (OEM) facilities and subcontracting company factories. For these failure cases, all the background and technical details are available for accurate case classification.

The distribution of failure cases and failure sources represents mainly electronics assembly processes in the industrial, commercial, and medical electronics areas. The companies were mostly medium or large size. Therefore, different failure distribution data may be found, for example, in small-scale manufacturing, semiconductor, automotive or aviation electronics manufacturing processes, where the type of ESDS, construction, and handling of ESDS can vary. Component assembly phases have been fully automatized and most of the mechanical assembly operations were done manually, but fully automated processes are included as well.

5.2.1 Source of Failures

The failure cases are analyzed by using three categories; source, event type, and victim. The first category explains possible sources for failures based on the following items: static E-fields, ESD, EMI, *external power supply* (EPS), and a *high voltage* (HV) source. The observed failure sources with the percentage information of the total are presented in Figure 31.

The largest failure group in Figure 31 is ESD, which has been categorized when a direct ESD between the victim device and another object has caused the failure event. E-field is the source, for example, when an electrostatic force causes a failure. HV is selected when the voltage alone is the source of a failure. HV and EMI are categorized as the source when, for example, HV cable sparking generates EMI pulses, and the radiated RF noise disturb equipment operation. An interesting observation is that there are no major failure cases found where a charged human has been the source of the failure. This shows that EPAs built based on current standards can effectively prevent these kinds of failures.

EMI and problems with power sources represent together about 25 % of the observed failure and disturbance cases. Static E-fields and HV sources represent less than 15 % of the cases. This analysis suggests that a typical ESD control program may only partially cover E-field and ESD event detection, whereas HV sources and EMI detection can be easily overlooked.

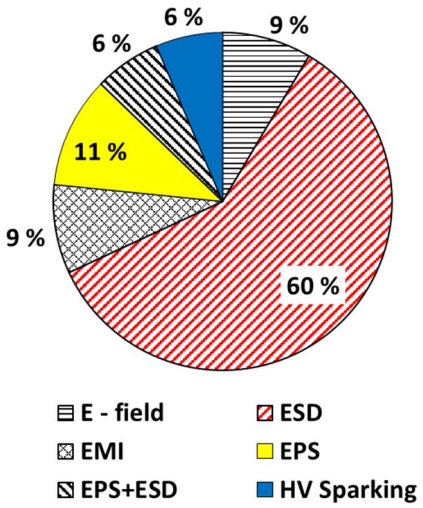

Figure 31. Observed failure sources.

5.2.2 Type of Failure Events

The second category shows a statistical distribution of failure event types based on the commonly used models: HBM, CDM, MM, CDE, *Latch Up* (LU), and CBE. These events involve electrical contact with charge transfer occurring. In addition, two additional event types are used based on *electrostatic attraction* (ESA) and failures due to radiated RF noise marked with EMI. The type and share of failure events are presented in Figure 32.

CBE is the most common failure event type shown in Figure 32. This is not surprising, as subassemblies, PCBs, and mechanical components are the most common parts handled in electronics assembly process. EMI events represent about one third of all the events leading to failures. This is consistent with several testing phases typically required during electronics assembly, programming, and qualification. The rest of the events represent each less than 6 % of the total. However, HBM, CDM, MM, LU, CDE, and ESA together cover about 20 % of all the failure events. Therefore, it is important to evaluate these event types when optimizing EPA control.

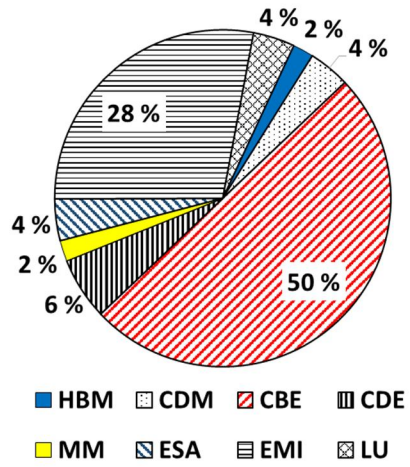

Figure 32. Event types leading to failures.

A high number of automated IC assembly operations has produced only very few CDM related failures. The data source used in this study includes billions of assembled components with less than 200 V CDM rating. The low number of CDM failures shows the low risk of ESD damage in the surface mount assembly processes used in most electronics assembly operations and supports the results presented in Chapter 5.4. In these processes, ICs are kept safely inside tape and reel packages until the IC is picked up by a nozzle for assembly.

5.2.3 Failing Components

The third category is the type of failing component in EPA based on the first and second category. However, it is not always as straightforward to define a single victim for a failure. For example, RF noise can couple via a cable and through several ICs on a PCB before it reaches the IC, which may finally produce the failure. Therefore, a specific IC has been selected to be the main victim only when failure analysis has proven the failure to exist inside the IC. In other cases, the victim is selected based on the module where the failure was observed.

Figure 33 shows that, in about 50 % of the failure cases, one specific IC in the product was found to be the main victim. The failure was due to a physical defect or a major electrical disturbance leading to a product failure. In addition, electrical testers and equipment have failed in about 20 % of the cases. This is once again related to the amount of EMI events and number of testing phases occurring in the EPAs

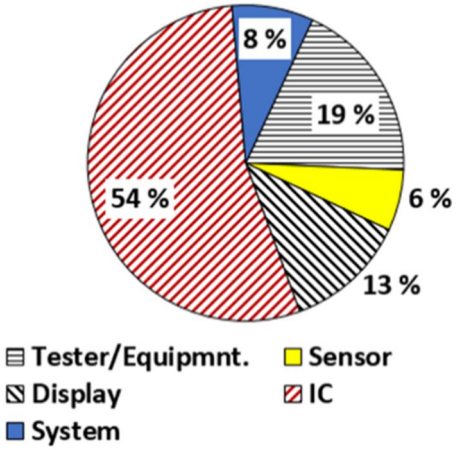

Figure 33. Failing components.

Displays and other electrical sensors have failed in about 20 % of the cases. Many of the electrical systems have a display or sensors integrated, and these can be susceptible to both ESD and electrical disturbances due to EMI. In electronic assembly, these components are still open and accessible for processing, which increase ESD and EMI risks. Displays also contain large dielectric plastic or glass surfaces that can be easily charged, for example, by peeling off a temporary protection film. These surface charges may trigger ESD or ESA events leading to product failures. The system failure group has been selected when the failure has been a complex combination of mechanics and electronics, and it has been challenging to define a single failing component.

5.3 Correlation of Component HBM and CDM Qualification Levels with Electrical Failures

100 V HBM limit is currently used as the base for building an EPA and ESD control program according to the IEC61340-5-1-2007 and ANSI S20.20-2014 standards [a]. ANSI/ESD S20.20-2014 offers an additional 200 V CDM limit and maximum 35 V limit for floating conductors. However, HBM and CDM qualification standards state that these should be used only to compare electronic component ESD robustness between different suppliers. In addition, the sensitivity of the subassembly is not the same as the sensitivity of single IC devices, as the IC device level information is valid only when the device is not soldered or glued on the system board. On a subassembly or system level, the ESD stress event can be very different, and sometimes the standard EPA environment can have major overkill with the protection principles [viii]. Basically, an EPA should be able to prevent ESD events leading to electrical failures, but ESD failures can still exist in EPA, as discussed in Chapter 5.2. In addition, electrical components with a low HBM and CDM withstand voltage would be expected to have, in principle, more electrical failures than more robust components. Here, the coverage and completeness of an ESD control program should also affect the *manufacturing failure rate* (MFR) [b].

The component HBM and CDM withstand voltages have been compared with ESD risks, field failure levels, and system-level ESD immunity in several publications, including white papers from the Industry Council on ESD target levels [1][31][32][43][55][91]–[93]. The White Paper I compared system-level field failure rates with the single component HBM withstand voltages [1]. The data consisted of field failure returns for 21 billion devices with the HBM sensitivity of more than 500 V and shows no correlation between the HBM sensitivity and field returns. A similar study was carried out for the CDM withstand voltage data in the White Paper II [31]. This document presents statistics for 9.5 billion components and shows no correlation between field returns and the CDM sensitivity when the CDM withstand voltage is between 100 V and 2 kV. Some publications indicate higher field returns when the CDM sensitivity is less than 500 V [31][92]. There is less published information available on how the HBM and CDM withstand voltage correlates with the MFR.

HBM and CDM withstand voltage information are compared with electrical failure levels in an electronics assembly in the reference publication [b].

5.3.1 Source of the Data

An IC is reported to have an electrical failure when a tester has measured a specific component parameter to be out of the accepted range and when a component replacement in a rework has restored system functionality. Other failure types, such as mechanical defects, are not part of the statistics. However, there are always failures that are difficult to classify, and the exact reason for failures has some uncertainties. Full failure analysis is typically done by component suppliers only when a significant number of similar failures occurs in electronics manufacturing or the component has a high-quality requirement.

The MFR data is based on 47 different products with a total manufacturing volume of about 150 million units between 2007 and 2015. The products were manufactured in 14 facilities having an automated surface-mount assembly, manual and robot-based final assembly, testing, programming and final packaging operations. Part of the data bases on the same information is used in Chapter 5.2. The facilities are located in Europe, Asia, and South and Central America. A total amount of different ICs handled during this period was about 6 billion. From these products, all ICs were used during a preselection phase to analyze MFR and ESD sensitivity data. Finally, 37 ICs were selected for detailed analysis based on the ESD sensitivity, availability of ESD sensitivity data, and reliability of the electrical failure reports. Most IC components with the 47 products had the ESD sensitivity equal to or more than 2 kV HBM and 500 V CDM.

Out of the 37 components, 13 were used in several products during the same period. In addition, one product could have one to six similar components on each PCB; thus, the total tested component count for the 37 ICs is about 1.5 billion. Fifteen components out of 37 have the ESD sensitivity less than 500V HBM and 500V CDM. The most sensitive components have the HBM withstand voltage 100 V, and six components have CDM sensitivity equal or less than 250 V. These most sensitive components are RF devices directly connected to antennas with an operation frequency between 700 MHz and 6 GHz.

5.3.2 Failure Analysis

Component HBM and CDM withstand voltages are compared with average electrical failures in Figure 34 where letters represent different IC components. The figure shows that most components have electrical failure values below 50 *parts per million* (*ppm*), and only five out of 37 components have over 100 *ppm* values. The highest *ppm* values are with components *q* and *r*, where the failure symptom is not ESD-related, as the damages were related to software problems in a tester. In addition, the failure rate with components *s*, *t*, and *a* is not related to ESD damages but to other EOS events leading to thermal damages.

Based on the collected monthly level statistics from all ICs and the 37 ICs shown in Figure 34, there is no correlation between the electrical failure data and component HBM or CDM withstand voltages. Both the ESD sensitive and ESD robust components can have low or high *ppm* levels depending on the case. However, the challenge with long-term failure data is that EOS events leading to electrical failures may not occur with a steady rate or at a rate that makes the failure level visible. This is also the case with random or short-period ESD failure events, which may not be visible in the monthly data.

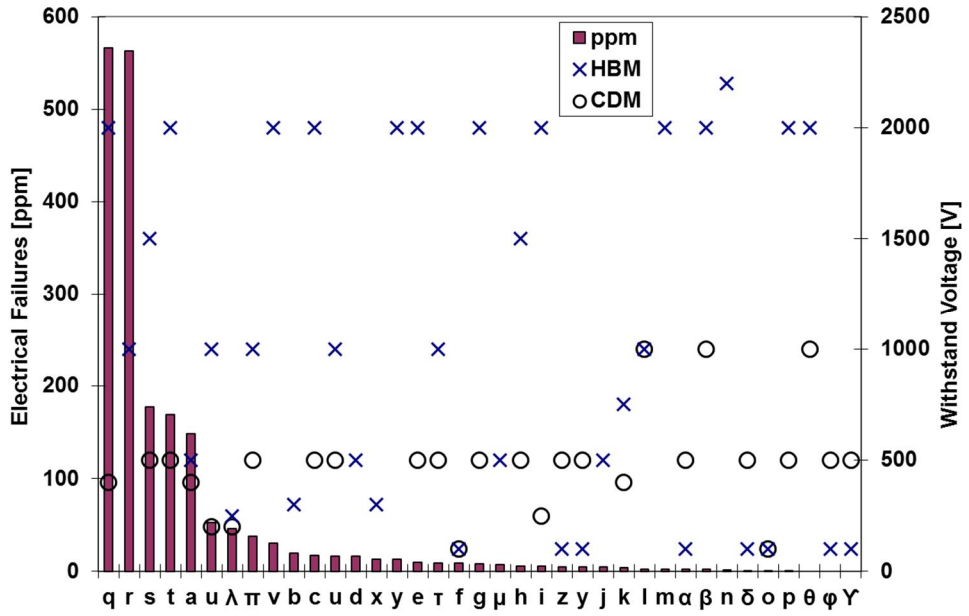

Figure 34. Component HBM and CDM withstand voltages and reported average electrical failures.

The same IC on a PCB can have varying electrical failure levels in different products. This is shown in Figure 35, where the monthly *ppm* level and the HBM and CDM withstand levels are presented for 13 components identified by letters. Columns with a same letter show the *ppm* levels for each product. The *ppm* level can vary between different products, even those that are produced on the same manufacturing line with the same tools and equipment. Here, the difference comes from varying PCB layouts, different mechanics used with the system, maturity of the assembly processes, and also from different testing methods and software used to operate the system. Once again, the electrical failures shown in Figure 35 are mostly not related to ESD events but include other EOS failures originating from latch up, test software, and component electrical failures due to system or component-package-level design issues. With these 13 components, there is no correlation with electrical failures and ESD withstand voltages—even the total manufacturing volume of products was counted in tens of millions.

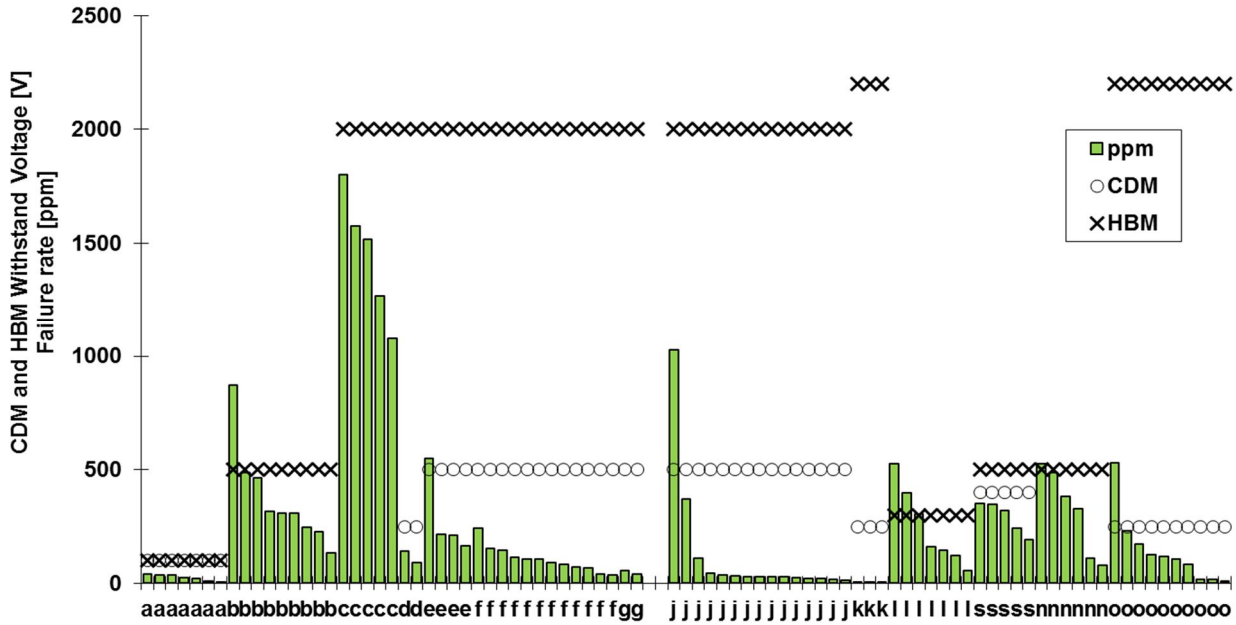

Figure 35. Component HBM and CDM withstand voltages and reported electrical failures between different products.

Similar to the long-term data, the weekly or daily electrical failure data show no correlation with the component HBM or CDM sensitivity data, as the reported ESD defects cases occurred both with ESD sensitive and ESD robust ICs. However, a majority of the found ESD events took place during the dry season with less than 45 % relative humidity in EPA [d].

A sudden increase in the electrical failure rate may be a signal of a possible ESD issue. In addition, the weekly or daily level quality data are able to prove the effect of corrective actions made on ESD control methods. This is shown in Figure 36, where EMI disturbances due to ESD events increased the electrical failure level from close to zero ppm up to about 450 ppm. An arrow shows the time when corrective actions were started. However, in the defect case, several corrective actions were required, such as changing dielectric packages to dissipative and purchasing new ionizers, which took several weeks to implement and to be effective.

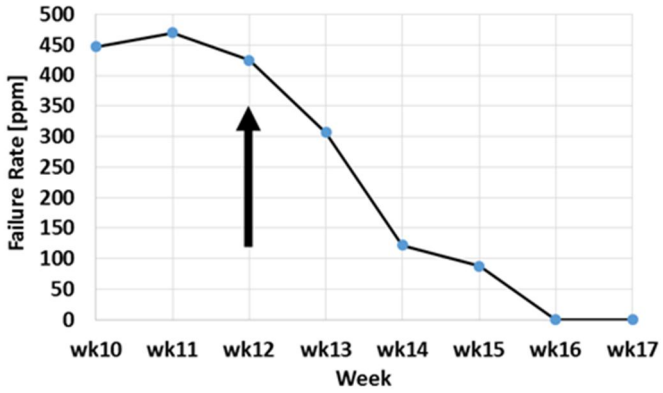

Figure 36. Weekly MFR data due to an electromagnetic disturbance.

5.3.3 ESD Control Program Audit Results Versus Electrical Failures

ESD audits were made for the same facilities between 2007 and 2015 from where the component electrical failure information was collected in Chapter 5.3, and the audit results are presented in Figure 37 [b]. The control programs were audited against ANSI/ESD S20.20 and IEC61340-5-2 standard requirements with additional requirements for the control of product specific ESD risks. All the audited facilities had a minimum of a basic ESD control program established, which included, for example, floorings with below 10^9 Ω resistivity, electrostatic conductive shoes, equipment groundings, wrist traps for the operators, dissipative plastic trays with most ESDS, and an ESD control program documentation. However, there were major differences with the level of control documentation, ESD responsible competence, compliance verification methods, and additional product specific control methods. These facilities had different process equipment and different products under manufacturing, but most of the facilities had the same 37 components in use.

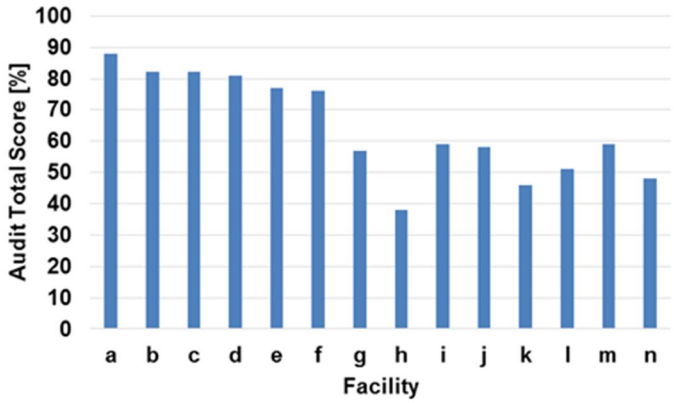

Figure 37. Facility ESD control program audit results.

There is no correlation between the ESD control programs audit scores and electrical failure rates. Instead, about half of the ESD sensitive components had actually higher electrical failure levels in facilities *a* and *c* than in

facilities with less than 60 % audit score. This is mostly explained by Figure 35 data, showing that the IC specific *ppm* level varies between different products and facilities. Still, most of the audited facilities had a major ESD defect or system disturbance cases leading to major financial losses during the data collection period. These events occurred in high- and low-ranked facilities, but there were not enough failure events to use it for additional statistical analysis. Most ESD failures occurred with I/Os in multifunctional large processors and control ICs having multiple connections to other components, subassemblies, and user interface connectors. These defects are included in the electrical failures and disturbance cases shown in Chapter 5.2.

5.4 Surface Mount Assembly

The main focus with ESD control in electrical component assembly has been with CDM risks. HBM risk level is low, as single IC devices are not handled manually due to automated assembly phases. In addition, ICs are typically not touched by the operators due to an increased contamination risk, and, for example, in the rework phase, operators use vacuum pick-up tools or tweezers to handle single components. Therefore, component placement process is the only phase during the electronics assembly where a single IC touches another surface, a resistive solder paste. These processes are typically kept well under control, and very few CDM ESD failures have been presented in publications when compared to the huge amount of IC components actually assembled [d]. Therefore, a CDM discharge from a single IC is a more realistic scenario in a wafer manufacturing, back-end processing and tape and reel packaging where wafers and single ICs are handled by several process steps.

The rest of the manufacturing phases in an electronics assembly contain more or less only assembled PCBs and subassemblies; thus, CDM events similar to the CDM tester environment are difficult to reproduce. However, there are publications reporting similar electrical component damages as found in a CDM qualification [31][36][37][43][49][50][58][78]. This can be explained with fast discharges having similar peak current and pulse rise time characteristics as found with CDM. These discharge waveforms can be produced also by CDE, CBE or high-voltage HMM type of events.

Automated surface-mount assembly lines have had few major ESD failure cases despite of the found static charges on PWBs and ICs. Large-size PCBs, such as computer motherboards, typically do not charge more than tens of volts, as those require steady support tools, which will ground the board during assembly. Smaller-size isolated PWBs in a larger panel, such as mobile phone boards, have commonly static voltages up to hundreds of volts during handling, but the stored charge is typically only from a few up to 20 nC due to the smaller physical size. Still, charged PCBs can typically be found in multiboard panels, where single PCBs in the middle of the panel are not contacted by the process equipment as often as the PCBs at the side area.

CDM discharge risks in an assembly phase are studied in publications [e][i][ii][31][50][93]. In this process, phase single ICs and PCBs are handled with conveyors, grippers, clamps, vacuum nozzles, and component feeders. ICs are typically kept in a closed ESD safe reel and tape or tube package until those are picked for assembly. However, ICs typically have a dielectric plastic, metallic, or ceramic encapsulation, and there are triboelectric charges in components after pick-up. Figure 38 shows an example nozzle and component package potential levels measured in a Fuji CP6 placement equipment when components have been picked and kept by the vacuum nozzles [e]. This equipment is able to pick up and assemble 10 IC components in a second. The electrostatic quasi-static potential level can be hundreds of volts depending on the electrical properties of component encapsulation and ESD safe tape package materials. Here, even a dissipative material cannot prevent static charging, as the IC encapsulation has dielectric materials.

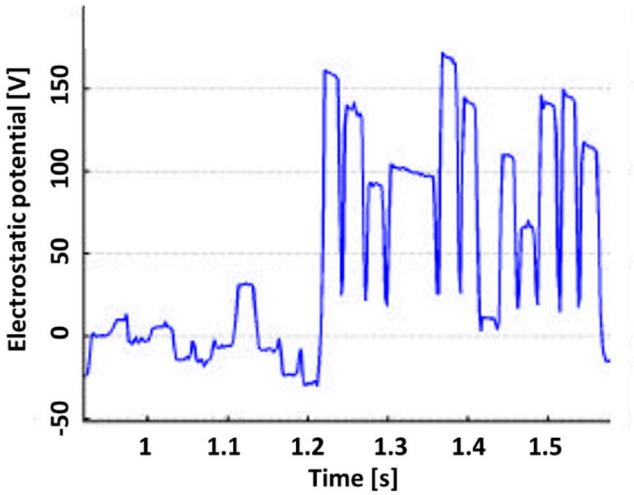

Figure 38. Electrostatic potential of nozzles (low peaks) and 12 IC components (high peaks) during a pick-and-place sequence.

Most publications measuring discharge currents during placement phase have used a pogo pin to contact ICs prior to assembly on the PCB. In addition, the IC has been charged with a high voltage source; thus, the PCB and IC have had a fixed potential when the discharge event occurs. In this case, the assembly scenario is not exactly the same as found in the real life.

When two charged conductive objects move closer to each other, the potential of the objects changes due to a change of the capacitance. Objects are capacitive coupled to the ground C_1 and C_2, and each other C_3 based on Figure 39. The potential difference between the approaching objects is now a product of the charges and capacitances. If the capacitive coupling is strong just before a discharge, the potential difference between the objects may be low, and a destructive discharge may not occur. This phenomena can be simulated with equations (12)–(16). Here, C_{ESDS} is the capacitance of the ESD source capacitance, and C_{PCB} is the capacitance of the floating PCB. The IC package and leads have different height affecting the capacitive coupling between the IC and PCB, as shown in Figure 40. This is simulated with the capacitance C_3. In the equations, it is assumed that the IC has an initial static charge Q.

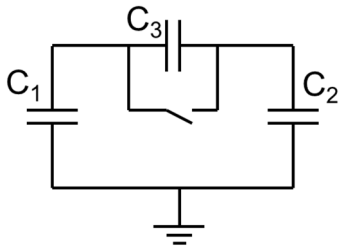

Figure 39. An equivalent circuit for a component assembly.

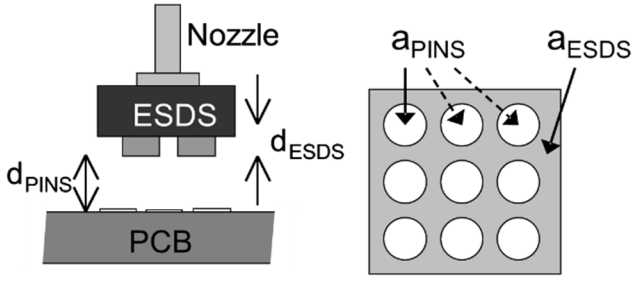

Figure 40. IC assembly scenario.

$$C_{ESDS} = C_1 + \left(\frac{C_3 \cdot C_2}{C_3 + C_2} \right) \quad (12)$$

$$C_{PCB} = C_2 + \left(\frac{C_1 \cdot C_3}{C_1 + C_3} \right) \quad (13)$$

$$C_3 = \left(\frac{a_{pins} \cdot \varepsilon_0 \cdot \varepsilon_r}{d_{pins}} \right) + \left(\frac{\left(a_{ESDS} - a_{pins}\right) \cdot \varepsilon_0 \cdot \varepsilon_d}{\left(d_{ESDS} + d_{pins}\right)} \right) \quad (14)$$

$$V_{PWB} = \frac{Q \cdot C_3}{C_{ESDS} \cdot (C_3 + C_{PCB})} \quad (15)$$

$$E = \frac{\left(V_{ESDS} - V_{PCB}\right)}{d_{PINS}} \quad (16)$$

Equations (12)–(16) were used to calculate *E*-fields and the CDM discharge potential levels for LGA, PLCC44 and DIL8 components shown in Figure 41. These represent different CDM scenarios, as the length of the pins d_{ESDS} varies from 0.3 to 6.36 mm. Detailed analysis are presented in the reference publication [e].

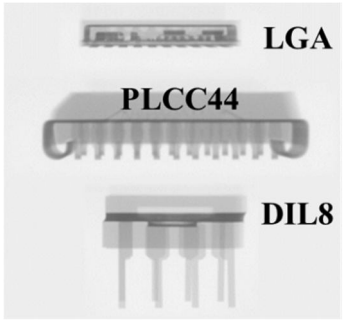

Figure 41. X-ray image of the LGA, PLCC44, and DIL8 packages.

The realized CDM discharge voltage V_{CDM} is the potential difference between the V_{PWB} and V_{ESDS}. A CDM air discharge can occur when a distance between the ESDS and PCB is more than a few micrometers. A Paschen curve predicts a minimum gap breakdown potential of 330 V at a gap of several micrometers and atmospheric conditions. With submicrometer gaps, the Paschen curve will not apply, and an air breakdown may still occur [17][94]. In addition, sharp objects can decrease the minimum gap breakdown potential due to a higher electrostatic field density. Therefore, it is challenging to predict exactly at what E-field density the air spark will occur between the IC and PCB.

Two cases are simulated: placement of a component on a grounded PCB and placement of a component on a floating PCB. The LGA component has an initial static charge Q=380 pC and capacitance C_1=0.36 pF. The potential of the IC V_{ESDS} is decreasing close to 10 V, according to Figure 42, when the LGA moves closer to the surface of the PCB due to the increasing capacitance C_{ESD}. At the same time, the electrostatic field between the objects increases and is about 200 kV/m with a distance of 0.05 mm. The potential difference V_{CDM} between the PCB and LGA, however, is then only about 10 V and is less than required to launch an air discharge. Therefore, severe CDM type of air discharges cannot occur with the simulated initial 1 kV potential and 380 pC charge level.

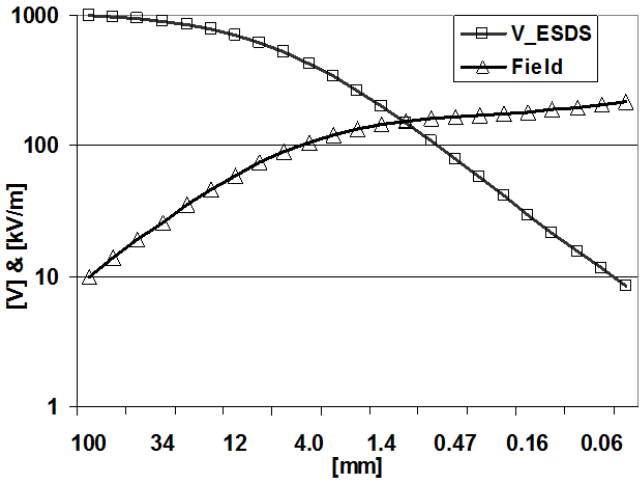

Figure 42. LGA package placed on a grounded PCB.

On a simulated floating PCB case, the PCB has an initial capacitance C_2=10 pF to the ground reference planes. According to Figure 43, potentials of both the LGA and PCB will approach the same value V_{CDM} =37 V when the distance decreases. The electrostatic field between the LGA and the PCB stays well below 3000 kV/m, and severe CDM type air discharges cannot occur with the initial charge level.

The simulated and measured voltage drops are less with PLCC4 and DIL8 IC components. However, there are more uncertainties related to the calculated potential and E-field values due to the more complex shape of the components. With the PLCC44 the V_{CDM} is now about 120 V with a distance of 0.1 mm. With the DIL8, the potential V_{CDM} is about 500–600 V and the E-field is above 3000 kV/m at 0.2 mm distance; therefore, an air discharge is expected to occur before component contacts the PCB; thus, components with a few long leads have a higher CDM risk level when charged. More detailed analysis can be found in the reference [d].

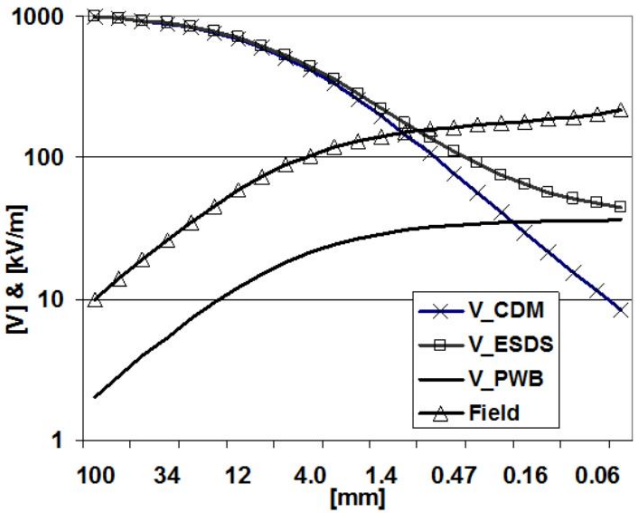

Figure 43. LGA package placed on a floating PCB.

Measurements trials with the three components were used to verify calculated results. The LGA component was charged via a contact up to 1450 V, and a parallel ground plate was moved to 0.2 mm distance from the component joints (time: 40 s – 60 s in Figure 44). The potential of the component was then less than 20 V, as presented in Figure 44. The metal plate was raised up, and the potential of the component was close to the same as before plate movements. This indicated that there were no air discharges between the ground and LGA due to increase of capacitances. This supports the calculation results shown in Figure 42.

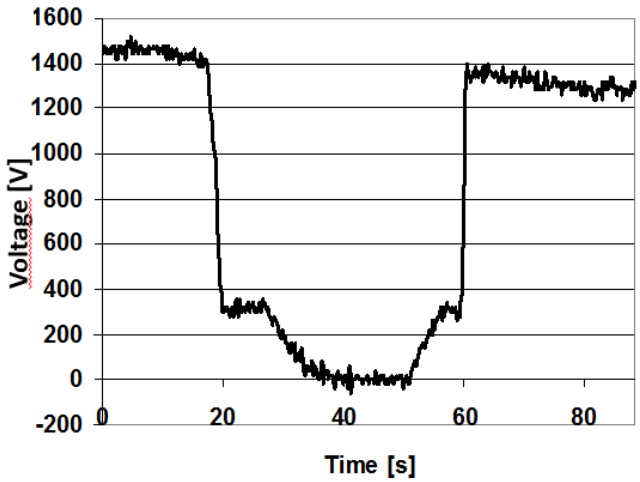

Figure 44. Potential of LGA package.

Similar results were obtained by placing a charged LGA directly on the surface of the ground plate. The initial 1500 V potential of the LGA decreased close to 0 V without any clear fast drop of voltages and EMI signal due to ESD event was not detected. Therefore, the CDM discharge at the moment of contact is well below 20 V.

When components approach a flat grounded surface, the drop of CDM potential is more than 95 % with the LGA, more than 85 % with the PLCC44, and about 40 % with the DIL8. The drop of CDM voltage between charged component and electrically floating PWB follows closely the same as if component would approach a grounded surface. Therefore, CDM risks depends on the type of the component package, and flat shape micro-BGA and LGA type of ICs have the lowest CDM risk due to a high-capacitive coupling. In addition, measuring the component charge or potential values before the assembly may not specify real ESD risks in assembly, but the charge value is more stable parameter for ESD risks assessment.

One more ESD risk type in an SMD line is the grounding of charged PWBs through ESD sensitive IC. For example, the conveyor in Figure 45 has green-color dielectric type of belts touching PWBs, which is able to tribocharge PCBs during handling. To limit charging, conveyors must have belts made of static dissipative material, as presented in Figure 29. There is typically an increased risk level of CBE type of discharges if the PCB or the equipment has static charges. This can occur, for example, when a conveyor system has a clamp or center support to hold PCBs during handling. In a reflow oven, the support is made of metal to withstand over 300 ºC temperatures, as shown in Figure 45. Actually, the reflow process is a good ionizer due to the high temperature, but the PCB is not yet neutralized at the entrance area. Here, the PWB needs to have a designed safe contact area where metal-to-PWB connections are allowed or ionizations must be used to neutralize charged PCBs.

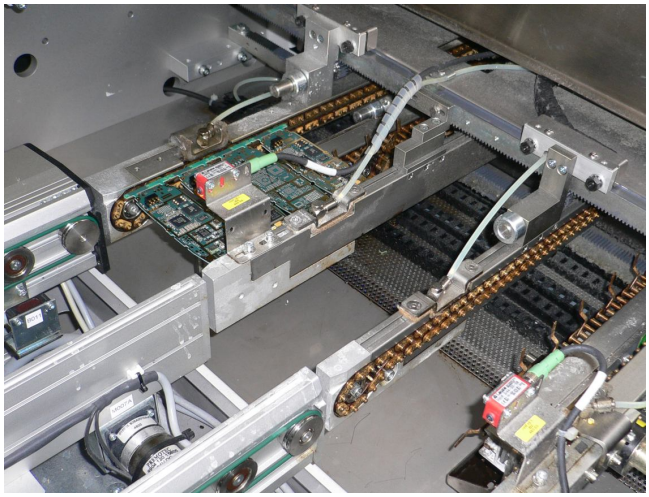

Figure 45. An entrance of a reflow oven with a metallic center support.

After the reflow single PCBs are separated from a large panel with routers, laser equipment, die cutters, and dicing saw methods. There is a risk of ESD in the case electrical signal traces are routed via the cut area. On top of ESD risks, an electrostatic attraction phenomenon can cause additional challenges in SMD assembly. Figure 46 shows an example case where lightweight ceramic capacitors are sticking on a top cover tape after the tape peeling. In this case, the top tape should be changed to dissipative material to limit charging of the plastic tape. An ESD control program in the SMD area can detect and prevent these failures with proper material control.

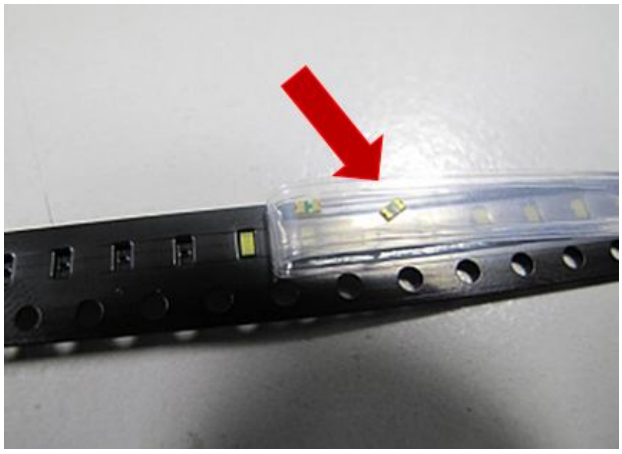

Figure 46. Component pick-up failures due to an electrostatic attraction.

5.5 Final Assembly

Chapter 5.2 has statistical information of the found electrical failures and disturbances in electrical assembly [d]. From these failure, cases around 80 % occurred in a final assembly phase, 20 % during a subassembly or product testing and programming, and the rest 10 % in a SMD assembly phase. This shows that final assembly phases are the most challenging processes to control from an ESD risks point of view in electronics assembly.

SMD processes are mostly similar with all electrical products, but FA is always tailored based on product designs. There can be several different versions of the final product where most of the changes are made by varying mechanical parts and software. A typical variation is made with product enclosures having different colors, markings based on the target customer, extra subassemblies providing additional functionality, and different external connections required by the customer. These are assembled manually, by robots, and with a combination of manual assembly and automated tools. Manual handling is the most challenging to control, as repeatability of assembly activities depends on the person making the work.

Even the FA is built according to the EPA requirements; however, there are still typically three major sources of electrostatic fields and charges; dielectric packaging materials used to store and transport mechanical and electrical components, dielectric components attached on the subassembly, and charged cable assemblies.

All electronic systems include dielectric materials that can receive triboelectric charges when contacted. For example, PCBs have a dielectric base material, and a dielectric solder resist covers most of the PCB surface. In addition, the outer surface of most ICs is made of dielectric plastic. A surface of displays is made of plastic or glass, and the display is typically covered with a temporary dielectric protection foil during FA phases. Therefore, display components can receive high triboelectric charges during handling. One more challenge is a discharge from a charged cable assembly [71][83][84]. Electric cables are covered with dielectric plastics, which charges and induces voltages on inner conductors. These and additional example ESD risks in FA are described in the reference publications [c] and [d].

A charged subassembly increases risk of ESD events; in this case, the assembly can be both a mechanical or electronic part. Therefore, it is not enough to focus only on charging of electrical components in FA. For example, when a charged display is connected with a PCB, the discharge can occur through some of the contact I/Os in a connector. These connectors typically do not have a designed ground pin that would contact at first when the

connection is made; thus, some of the ESD events can occur between sensitive I/Os. A discharge from a simple small metal part can also cause damages. For example, the metal part can be an antenna structure in a plastic part with kilovolts level of potential and a few nano-Coulombs charge [c]. This charge can discharge via the subassemblies when the plastic part with the antenna is connected with the electronics. The discharge waveforms can be similar to CDM and CBE; as the source capacitance can be a small metal object, there is only air spark resistance along the current path, and the serial inductance comes from the construction of the assemblies. Ionizers can be placed to process to neutralize charges, but this can be a too slow method, adds extra costs, and there may not be space available to locate ionization in an efficient way. Therefore, some amount of charges is still left in FA phases, and ESD risk need to be assessed based on the measured charge levels.

Figure 47 and Figure 48 presents the basic risk analyzing methods to detect ESD risks in FA phases. Potential and charge measurements show how much a product part or an adapter has static charges. The charge value is the only stable physical electrostatic quantity that can be measured with a measurement tool without changing the measured value when the measurement probe approaches the target. However, there are uncertainties with the charge measurement, such as the leakage current, which need to be under control [x][95]. In addition, ESD events can be detected or measured with EMI detectors [2][96]–[101]. Here, the EMI measurement tool can be a simple radio with an LED and voice alarm or a more complex system with antennas and an oscilloscope.

Figure 47. Contact charge measurement and EMI detection in an FA cell.

Figure 48. ESDS electrostatic voltage measurement.

Depending on the product design, there can be just a few or even tens of different additional parts to be assembled in FA phases. Dielectric packages are commonly used in the FA, as those are about two to three times more affordable than dissipative packages. All the dielectric packages have static charges on the surface and can induce potentials on non-grounded conductors influenced by the electrostatic field. An example FA environment is shown in Figure 49 where one single assembly station has four trays for mechanical and electrical parts.

Basically, ESDS components are stored in ESD safe packages until assembled. However, there are challenges with the quality of dissipative materials [2][vi][xii][88][102]–[104]. One example is shown in Figure 50, where a tray has more than 1 kV surface potential even it is purchased as a dissipative material, and the tray has a ground path via the dissipative green table mat. The challenge with materials is related to the unreliable qualification methods, with dissipative non-flat materials and long supplier networks providing similar packages with varying quality [2][103]. Therefore, additional process compliance verification methods and extra precautions are typically required in FA to fully prevent ESD risks.

One additional challenge with dissipative packaging materials is with the triboelectric behavior of materials. It is possible that a dissipative material will tribocharge subassemblies with dielectric materials more than a dielectric material [104]. The level of tribocharging can depend on minor differences with material properties. For example, there was a case where a product with a black plastic cover had major ESD failures in FA, but the same product with a white cover made of the same base plastic material never failed. In this case, the black plastic charged on dissipative trays whereas the white did not. The charged cover induced a potential on the PCB, and the product had a discharge when it was connected with a tester equipment via pogo pins.

Figure 49. A FA cell with multiple dielectric component trays. Ionizers are used to neutralize static charges.

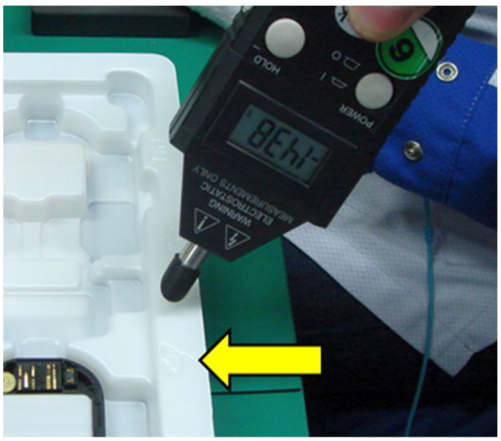

Figure 50. A charged tray with a dissipative package material mark.

5.6 Testing and Programming

Electrical testers and programming equipment typically make a physical electrical contact with DUTs. The contact can be created via pogo pins in an in-circuit tester, via specific test interface connectors and via product-user-interface connectors, such as USB ports. In addition, the connections can be a combination of electrical and radio communication methods, depending on the DUT and process requirements.

Testing equipment can measure component or system operation parameters. However, depending on the type of the product and speed of the manufacturing, the test coverage can vary. For example, a basic current consumption measurement can be challenging to implement in a fast manufacturing process if the product runs complex software operations with fluctuating power consumption. Therefore, the measured parameters can have a high uncertainty, and alarm and failure limits need to be set wide to avoid excess false alarms. This can prevent detection of electrical failures, such as small leakage currents caused by EOS or ESD events [91][105].

Both the electrical testers and programming equipment can produce electrical failures [b]–[d]. Based on the collected defect and disturbance statistics, about 20 % of the failure cases in electronics manufacturing have occurred with DUT testing and programming [d]. Testing equipment can connect an external power source with the DUT, and wrong setup parameters or switching on the power in a wrong order may cause latch-up, overvoltage, and other EOS damages. In addition, if the DUT has a static charge when the electrical connection is made, the first metal-to-metal connection point will have an ESD event. A common discharge point is the electrical connection point where ground, power, and signal pins locate. In most cases, there is a low-failure risk level if the discharge occurs between the electrical grounds or power signals of the DUT and testing equipment. However, a discharge between I/Os can damage or disturb the DUT or testing equipment. These discharges can have significantly higher stress levels than component level HBM or CDM qualification tests [c][xi]. Some of the discharges can occur via on-board tests pads that do not have additional EMC/ESD protection, as those are not accessible when the system is assembled. Therefore, the local stress level can exceed IEC61000-4-2 qualification levels built for a complete system.

Testing and programming equipment are typically tailored in-house based on the DUT construction. Therefore, electrical connections between the DUT and equipment may not use shielded cables or connectors where the electrical ground makes the first contact; therefore, the exact EMC immunity and emission level of in-house designed systems can be unknown. In addition, some of the DUTs need to be connected on the powered state, which increases risks of EOS type of failure events and software disturbances due to EMI.

Figure 51 shows an example failure case where a CBE event disturbed operation of the programming station [c]. An EMI pulse was detected when products were placed manually on to the programming station. Products had dielectric plastic covers, which received triboelectric charges during handling. The charged covers induced an electrostatic potential on conductive parts of the electronics, and this charge was discharged into the ground when products were placed into the adapter. The EMI coupled into a nonshielded clock signal cable, and an example distortion, as shown in Figure 52, was measured with an oscilloscope. The raising edge of the clock pulse was lost and data transmission stopped. Similar EMI events caused more than 10 % testing yield losses in the manufacturing area before the case was solved by improving shielding of the data cables.

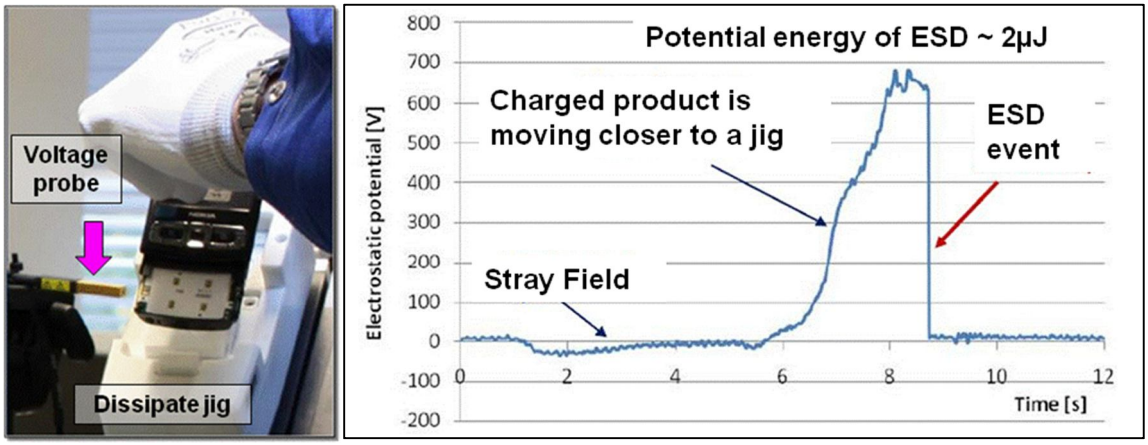

Figure 51. A discharge event in a product programming phase.

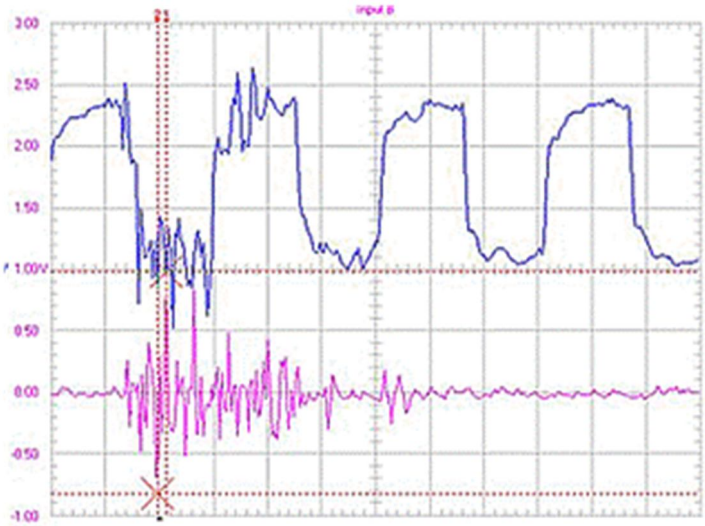

Figure 52. An EMI pulse and a distorted clock signal.

A charged jig, as shown in Figure 53, can produce similar ESD and EMI events, as if the product itself would have a charge. In this case, there is a discharge between the product and the jig. The test jig needs to have dielectric materials to isolate electrical connections, but large charged dielectric surfaces can induce a potential on DUT. These cases were fixed by changing major parts of the dielectric materials to a static dissipative. Similar ESD scenarios due to charged jigs and adapters have caused major yield losses in electronics assembly, testing, and programming.

Figure 53. A charged test jig with over 1 kV surface potential.

ESD events can also initiate latch-up and other EOS failure events by disturbing the operation of equipment. Figure 54 shows an example case where a programming equipment started to suffer electrical failure to a USB control card inside an industrial computer [d]. When a worker plugged a USB cable into a charged product, a CBE ESD went through the cable into the computer. Only one specific USB card model showed failures. In a short period of time, tens of cards broke, but the products under programming were still fully functional. This discharge was relatively weak, but initiated a latch-up phenomena in the USB card that led to damage to USB control circuits. The USB card had an unknown EMC/ESD design, and the primary corrective action was to improve EMC/ESD filtering with the data connection. The case was completely resolved by adding two low-cost snap-op ferrite cores along the USB cable.

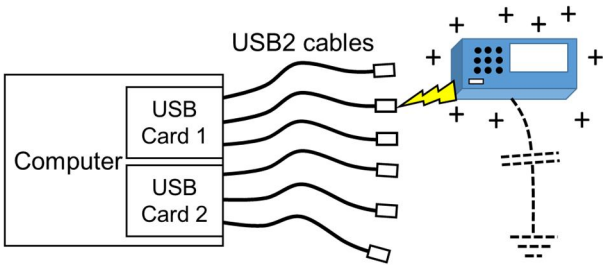

Figure 54. Latch-up failure triggered by an ESD event.

5.7 Rework

Rework operations are typically done on a workbench, such as that shown in Figure 55. The workbench can have varying measurement equipment and tools to identify and change failed components. Most of the ESD risks can be prevented with basic EPA rules by using low-charging materials and grounding all the conductive and dissipative items. However, a rework phase has to access electrical signals and test pads on the PCB during a system operation to analyze where a failure may locate. In addition, soldering and heating tools touches directly on ESD sensitive components when failed components are changed. There are also conductive jigs and adapters to hold PCBs and assemblies during the rework.

ESD failures have occurred in the rework phase, for example, due to a leakage current in a soldering equipment and due to charged products discharging into the test equipment or into conductive hand-tool.

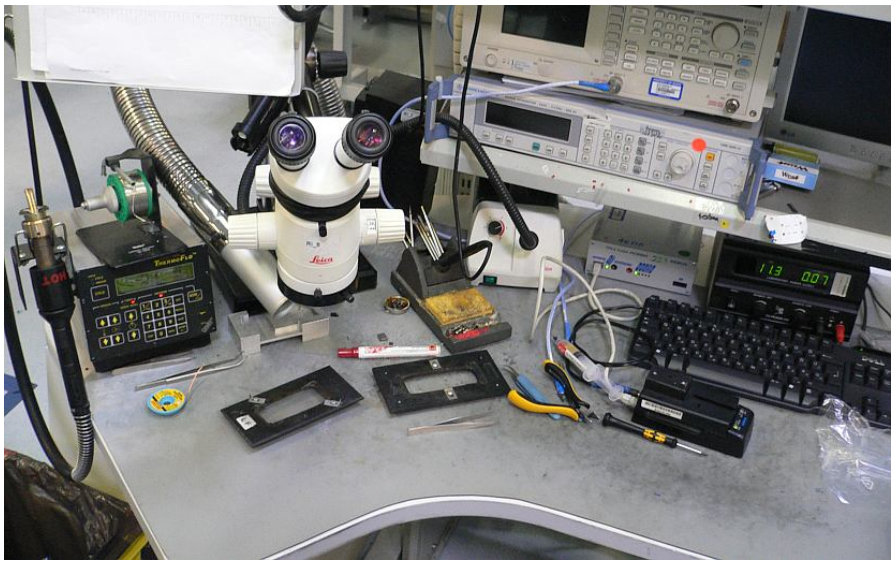

Figure 55. An example rework station.

6 Advanced ESD and EMI Control in Electronics Assembly

Based on analysis, current ESD control programs are not always able to prevent ESD damages in an EPA. On top of actual ESD events, there can be EMI initiated product and equipment disturbances in the EPA. Therefore, most of the additional control methods should focus on FA and testing process phases where about 90 % observed failure and disturbance cases have occurred. Of these events, CDM, CBE, and CDE discharge events cover about 60 % and equipment or product disturbance cases about 30 % [d].

In an improved ESD control program EMI detection, a product part and cable charge control are added into the program, together with groundings and other basic controlled EPA items. The program can be based on the existing ESD control methods wherein the main parameters to monitor are the groundings, material conductivity, static *E*-fields, and surface potentials. Charging of product parts should be monitored with potential, discharge current, and charge meters, and that data should be used together with process analysis to detect all known ESD risk scenarios, i.e., HBM, CDM, HMM, CBE, and CDE. Once again, these values cannot be directly compared with the IC level HBM or CDM qualification data. Instead, alarm and corrective action thresholds should be based on found ESD and EMI disturbance events and set based on the real product and equipment immunity tests. These advanced control methods can produce significant cost savings with optimized investments and process control methods [viii][xii][106].

Measuring and controlling dynamic ESD and EMI events requires additional nonstandardized tailored measurement tools and methods and also broader personnel training and competence. On the other hand, there are fewer items to monitor on the dynamic electrical events level, when compared, for example, with EPA groundings and material verifications. This is shown in Figure 56 where the control program and typical controlled parameters are presented with three layers [a].

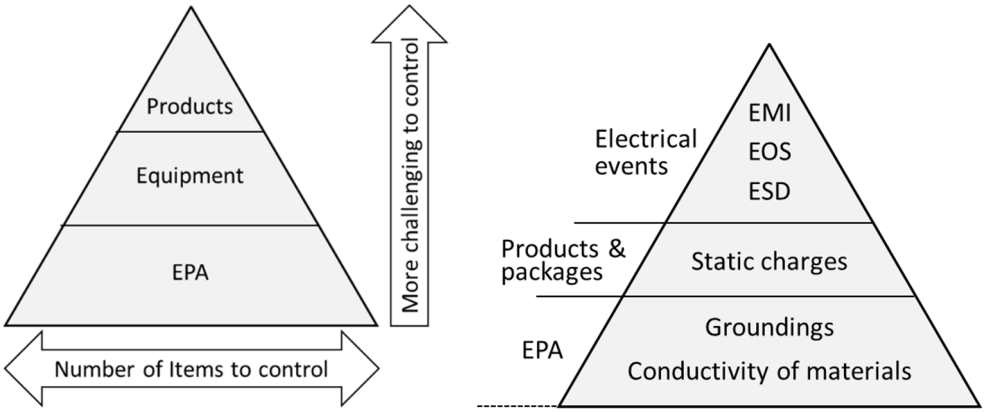

Figure 56. Three layers of controlled items and parameters in an advanced ESD control program.

Taking the varying discharge environment into account can be a major benefit with product level risk analysis. A drawback of this principle is the fact that product-specific ESD risks and sensitivity is valid only in the specified process and needs to be analyzed separately each time the process or product will change. A basic assumption for the detailed risk analysis is that the process is in an EPA where, for example, personnel and equipment groundings exists.

6.1 Phases of the Risk Analysis

Process and product risks are analyzed step by step as follows [a][c]:

1. **Analyze target processes to find possible ESD/EMC risks.**
    - Define the process critical path where ESD sensitive assemblies are handled.
    - List all those phases where CDM, CDE, or CBE types of scenarios are possible. List all EMC noise sensitive process phases.
    - Define a risk map with risk-analyzing methods.

2. **Select the high-risk processes for further analysis.**
    - Analyze discharge contact parameters (metal-to-metal contacts) and dynamic capacitance of a charged object during a discharge event.
    - Measure E-field, EMI, charge, and potential levels in each selected phase.
    - Measure discharge environment parameters: capacitance of the ESDS, capacitance of other objects coming in contact with ESDS, and resistance of ground paths. Estimate discharge peak currents with sample measurements.
3. **Build discharge test setups based on the measured discharge environment parameters.**
    - A test bench is built by using metal plates and dielectric or dissipate sheets [4]. It can be also possible to use real product specific adapters or jigs in a test bench, but often those items cannot be removed from the process.
    - Use simulations and calculations to verify the stress level.
4. **Stress one to three DUTs with selected potentials and charge levels on the chosen contact points.**
    - The discharge must be made in a similar way as occurs in the real world process. The best accuracy can be reached when discharges are made with the real contact item such as a wire, a mechanical part, or another ESDS. The discharge can also be made with a ground wire having chosen RLC parameters to measure discharge current with a current clamp.
    - For EMI sensitivity analysis, collect long-term operation data and record the strength of pulses.
    - It is not necessary to stress all DUTs up to a failure level, as testing can be stopped when the stress level exceeds the maximum levels found in the process area.
5. **Specify product part ESD sensitivity.**
    - Use the discharge waveform information or quasi-static parameters that the test bench provides. For example, a *field induced charge board event* (FICBE) [c][31] and FCE methods provide capacitance, potential, charge and energy information, and optionally a current waveform data. A TLP provides an IV data plot, pulse rise time, and energy content information.
    - Define the corrective action and alarm limits based on the potential and charge values. Use the discharge current information when available. Define limits for the maximum allowed EMI pulses.
    - Define the generic warning and safe process limits based on the results.
6. **Report the alarm and warning limits to process responsible. In addition, inform R&D if the product sensitivity is found to be at high-risk level.**
    - Specify in which process phase(s) the limits are valid.
7. **Follow the handling processes.**
    - ESD responsible shall monitor processes based on the alarm and warning limits.
    - Corrective actions are made based on the measurement results and process yield data.

6.2 Analyzing the Target Processes

To define the process phases with the highest risk can be challenging. However, ESD risks in electronics assembly operations can be analyzed with *design failure modes and effects analysis* (DFMEA) methods [b].

ESD risks can be analyzed with stochastic processes, which involve a sequence of random variables and the time series with the variables [107][108]. ESD events leading to damages in these phases can be dependent, partially dependent, or independent of each other. For example, a product assembly may get triboelectric charges in a process phase where the device is picked up from a tray. In the next process phase, the device is contacted with a conductive metal object, thus discharging the charge and possibly causing damage. Here, the process phases work independently, but both are required to realize the ESD event. Mitigating the ESD risk can be done in either process phase, but the best result would be obtained by preventing both the charging and discharging event.

The total failure probability of an assembly line or a system P_t can be expressed as

$$P_t = g\,(F_1, F_2, \ldots F_n), \qquad (17)$$

where function $g(\bullet)$ describes the relationship of each event F_i [107].

Each event in the process can be expressed by its parameters $F_i = f_i\,(x_1, x_2, \ldots x_n)$, (18)

where x_{in} define affective parameters for each function. These parameters x_{in} have a certain variation and uncertainty; thus, the event F_i is not constant. When all the affected parameters x_{in} are known, the F_i can be calculated. In addition, it also may be possible to estimate the events directly by using statistical data collected from the process. A product of the events will give the total failure probability P_t.

Figure 57 show typical functions and parameters estimating the probability of an ESD failure event based on equations (17) and (18) for an automated electronics FA line, as shown in Figure 2. In addition, the realized risk level can be estimated with an additional function, including the failure severity or consequence of the failures. The functions can be explained with time domain probability expression information, as shown in the example data set in Table 4. In this example, the step number 6 is a final assembly phase where a charged tablet display is connected with a PCB. This step has an increased risk level to damage either the display driver IC or the display itself due to a CBE discharge. The display flex connector, measured potential, and charge values can be seen in Figure 58. Here, the flex connector is a push-in type where the first electrical contact can occur through any of the I/Os.

In addition, step number four has a small change for discharges in a PCB testing phase if the PCB has static charges. These two steps would need product ESD sensitivity analysis to clarify if the product can fail during handling, and preventive actions can be decided based on the sensitivity information and found charge levels in the process.

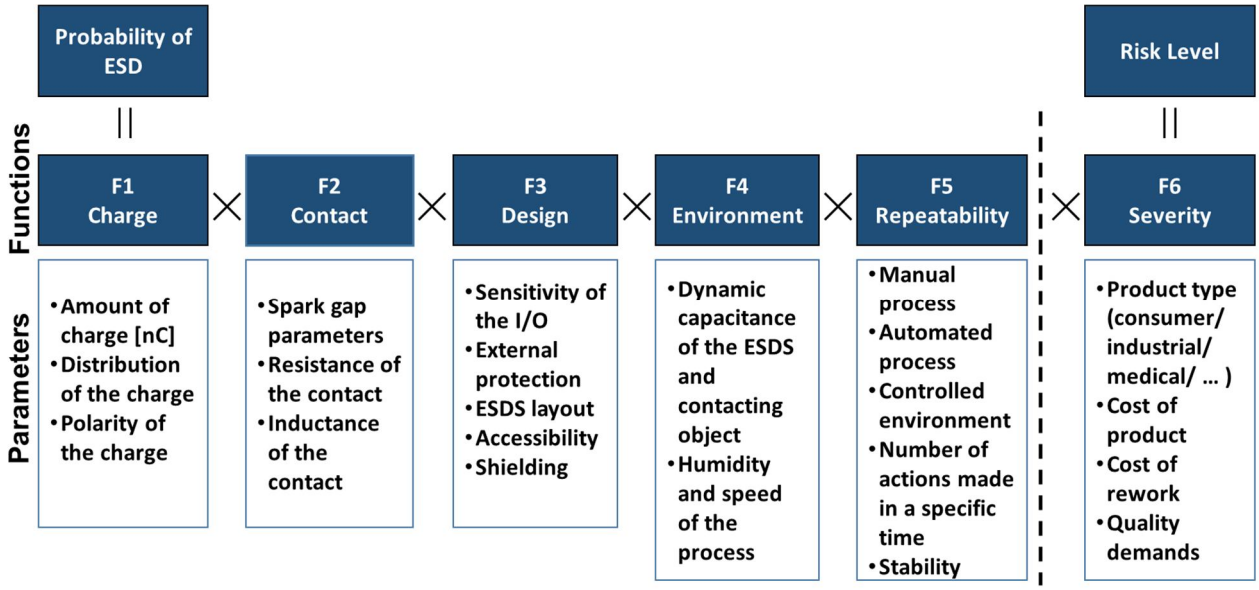

Figure 57. Functions and parameters affecting on the ESD probability and realized risk level.

Table 4. An example calculation of ESD failure probability for the ten steps based on Figure 2 layout and Figure 57 functions.

	1	2	3	4	5	6	7	8	9	10
Charge	0 %	0 %	0 %	5 %	40 %	20 %	10 %	5 %	0 %	0 %
Contact	0 %	0 %	100 %	100 %	0 %	100 %	0 %	0 %	100 %	0 %
Design	0 %	0 %	50 %	50 %	100 %	100 %	100 %	0 %	0 %	0 %
Environment	100 %	100 %	100 %	100 %	100 %	100 %	100 %	100 %	100 %	100 %
Repeatability	100 %	100 %	90 %	90 %	60 %	70 %	100 %	80 %	100 %	50 %
Defect Probability	0 %	0 %	0 %	2 %	0 %	14 %	0 %	0 %	0 %	0 %

Figure 58. A display flex connection phase in process step number 6 with a higher ESD risk level. The display assembly has a static charge of about 100 V and 20 nC.

6.3 Measurements in the Manufacturing Process Area

Electrostatic field, potential, charge, and EMI pulse control in electronics assembly requires tailored measurement methods. These methods, together with a discharge current measurement, have been found to be essential methods in providing information for ESD risk calculations; therefore, some measurement examples and methods shall be discussed [2][31][47][59][100][101][109]–[112].

Potential measurements can be made with electrostatic field meters, high impedance contact voltmeters, and with noncontact voltmeters. Charge measurements can be made with a laboratory electrometer, handheld Coulomb meter, or by integrating the charge from a measured discharge current data. EMI pulses can be detected with portable radio receivers (EMI detectors) or by using antennas and an oscilloscope [c]. Discharge current measurement is the most challenging control method, as ESD waveforms require typically more than 1 GHz bandwidth tools with a high current capability for accurate event capturing.

Electrostatic potential measurement in a process area can be made with battery-operated handheld voltage meters, such as with TREK520 and Infinitron 821 HH or by using E-field meters, as shown in Figure 59. These tools can measure DUT voltages with reasonable accuracy in a field environment. The accuracy of the reading depends on the size, shape, and material of the object to measure. In addition, the electrostatic field from the charged object is typically not uniform, and the shape and distance of the measurement tool can affect the measured voltage value [102]. A contact voltmeter is typically the only tool giving more repetitive results for small metal objects, such as with single ICs [93]. This tool has been designed with a low-capacitive coupling between the target and the probe tip.

It is challenging to measure exact surface potential values from a dielectric object. However, the surface potential of an insulator is typically not as valid a parameter for ESD risk assessments as it is the E-field from the charged surface, which can induce potential on non-grounded conductors. Therefore, a field meter is typically a better tool to estimate ESD risks from charged dielectrics, as it can measure the strength of the E-field (*V*/*m*) at the position of ESDS. This gives more accurate information for ESD risks assessments than measuring the E-field at 2.5 cm (1 in.) distance from the charged surface.

Figure 59. Surface potential measurements in the FA process area. The Trek520 on the left and middle. An electrostatic field measurement on the right side.

Charge measurements, as shown in Figure 60, with a handheld Coulomb meter and a contact probe are, in most cases, an accurate enough method to control product assembly charges [x][95]. With this method, a conductive part of the DUT is contacted with a tip of the probe. The contact will discharge charges of the DUT and inform directly a total charge of the object. However, this method cannot be used if the measurement setup has such a high current leakage that the measured value is not stable within a few seconds period. In that case, more accurate results can be obtained with a measurement method where the charge is integrated from a discharge current waveform within micro- or nanoseconds period [c][110][115][116][117]. This measurement method will also take into account a dynamic capacitance of the object; thus, the measured charge value has less uncertainties due to the small leakage and can better represent the real dynamic discharge scenario. Based on the potential and charge measurement, the capacitance of the charged objects can be calculated by using equation (1).

Figure 60. Product charge measurement with a handheld charge meter and a contact probe.

Electromagnetic pulses can be measured with an oscilloscope and antenna or detected with radio receivers, as shown in Figure 61. In addition, the type of the discharge and discharge location can be measured with calibrated multiple antennas [c][d][96–100]. However, there are typically non-ESD related EMI sources in electronics assembly, and distinguishing a real ESD event from other disturbances can require additional analysis with potential and charge meters. Here, small portable EMI detectors can help us to locate the process phases where EMI pulses originate. This is shown on the right side in Figure 61, where a Sanki EMI locator is used to detect possible ESD events beside an assembly jig with a charged surface. To link the source of an EMI to an ESD event typically requires several repetitive pulse captures; here, a video recording has been found to be an effective method.

Figure 61. EMI detection with an oscilloscope, TEM antenna, loop antenna, and EMI locator.

It is challenging to specify any specific control limits for maximum allowed EMI signal amplitudes in EPA [101]. It is possible to use calibrated antennas with a known frequency response to measure EMI signals, but the exact EMC immunity of process equipment is typically unknown. Therefore, one option is to collect history data of the measured EMI pulses and equipment disturbance cases and set alarm limits based on this information. In that case, the EMI measurement method and measurement distances must be specified in detail. One example alarm limit found applicable in several facilities is based on a simple 30 cm loop antenna connected to a 50 Ohm oscilloscope input. When the antenna is placed close to EMC noise-sensitive equipment, the maximum coupled peak voltage must stay below 0.5 V. A loop antenna works still well below 500 MHz where, typically, a major part of the EMI pulse energy is located. A wideband TEM antenna can capture RF noise with higher accuracy and can be used to set the maximum amplitude for detected EMI signals.

6.4 Subassembly ESD Sensitivity Tests and Simulations

Target of product-specific ESD risk analysis is to obtain practical information for handling, manufacturing, and R&D purposes. The risk level depends on the sensitivity of the products, which can be the maximum stress level products can withstand in the worst-case environment. The sensitivity can be validated also in a fixed discharge environment, in a similar way as with component level HBM and CDM validation. Another option is to specify the sensitivity as a maximum stress level the product can withstand in a real discharge event found in the handling and processing environment. This real-case option is more efficient, as products are typically not stressed in EPA with the worst level stress. The worst-case scenario would most likely lead to overkill with ESD control precautions.

An extended control process needs to define practical and realistic warning and alarm levels for ESD and disturbance risk scenarios. For that aspect, the following procedure is proposed for the criteria [a]:

a. Define the exact warning and alarm limits only for specific ESD risk scenarios wherein normal ESD prevention activities would be challenging or expensive to deploy. This limits the amount of product testing required.
b. Define generic warning and alarm limits for all ESDS parts used in the process based on stress tests that simulate the real process environment.
c. Use a measured quasi-static charge and potential values with compliance verification measurements to control the CDM, CBE, and CDE risks.
d. Define criteria for maximum radiated and conducted EMI noise close to EMC sensitive processes.

The subassembly stress tests can be conducted with the test methods presented in the Chapter 4.5. The stress tests can follow the sequence of Figure 62, where the target is to find a level in which the DUT fails or the stress level exceeds the typical maximum level observed in the process phase [c]. It is recommended that at least three similar DUTs will be tested to clarify part-to-part sensitivity variation. In most cases, there are only a few contact points with metal-to-metal contacts in an assembly process. This limits the number of tests required. However, some electrical connectors may have tens of I/Os that require parallel testing, such as shown in Figure 63.

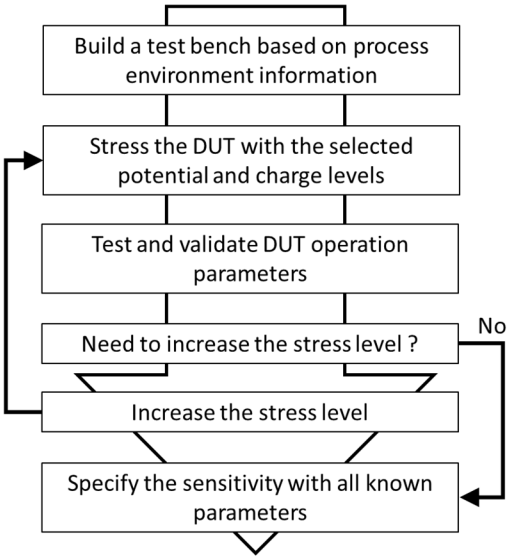

Figure 62. Product ESD sensitivity analysis.

Figure 63 shows an example stress test setup where the ESD sensitivity of the process step number 6 discussed in the Chapter 6.2 is tested by using the real product assemblies already shown in Figure 58. The CBE field induction test bench is constructed with dielectric sheets and metal plates so that the environment is similar to the real process assembly phase. Here, the display flex connector is discharged into the PCB via a 20 mm long wire with a CT6 current probe. The figure also shows the resulting current and the integrated charge waveforms with a 300 V pre-charge. With this level, the maximum measured and calculated stress parameters are I_{Peak} = 2.7 A, Q_{Total} = 12 nC, and E_{Max} = 1.8 µJ. The assemblies survive this stress level even when the charge and potential levels exceeds the values found in the real process environment. Based on the result, the process phase is safe, and no additional ESD protective actions will be required for the display assembly phase.

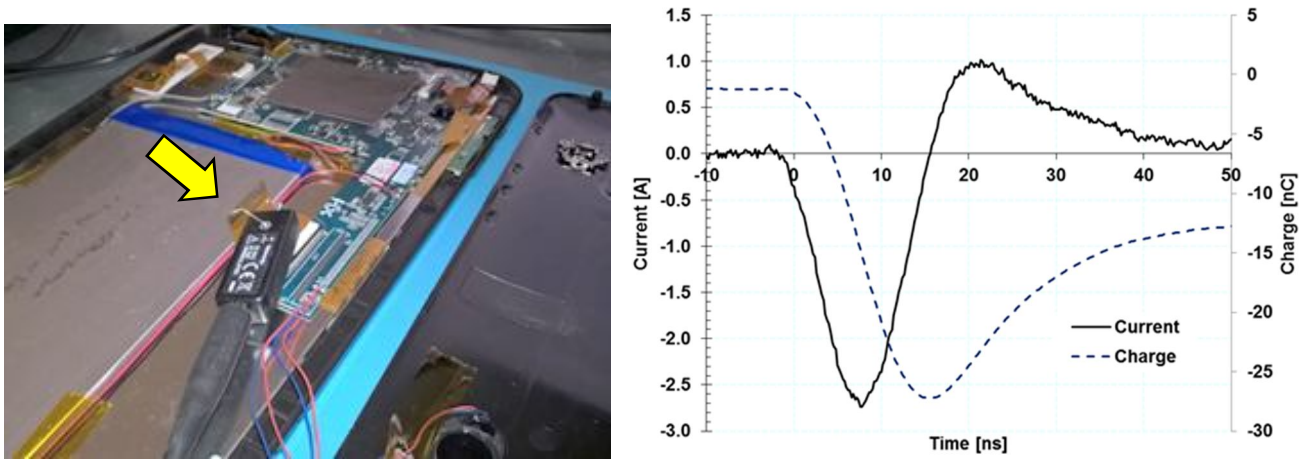

Figure 63. ESD stress tests by using field-induced charges. A calculated charge and the measured discharge current waveform between the PCB and flex connector are on the right side.

Simulation tools can be used to verify and fine-tune the measured stress parameters. In addition, simulations can provide additional parameters for R&D purposes of the DUT stress level [c][f][iv][ix]. Figure 64 shows example CBE test setups used in a CST Microwave Studio and SPICE simulation environment. Both methods can predict the discharge current waveforms when the environment and circuit parameters are known in detail. This is shown in Figure 65 where a complex simulated FCE current waveform has a good correlation with the measured DUT stress level in a test bench.

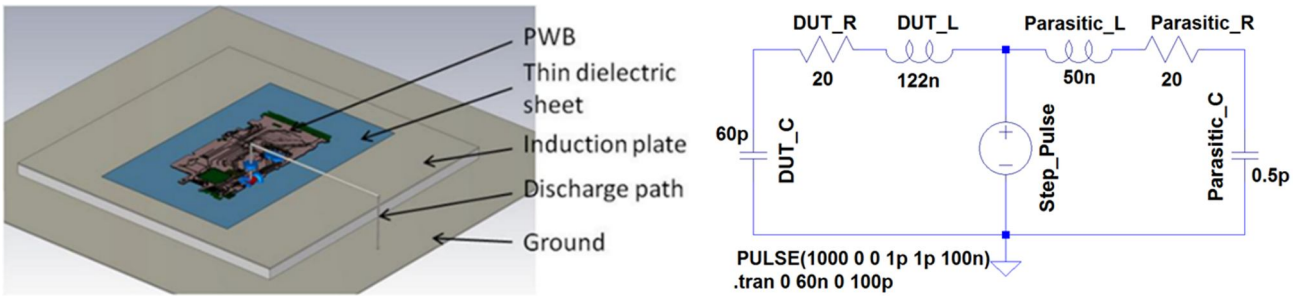

Figure 64. CBE simulation with CST Microwave Studio software and a SPICE simulation model on the right side.

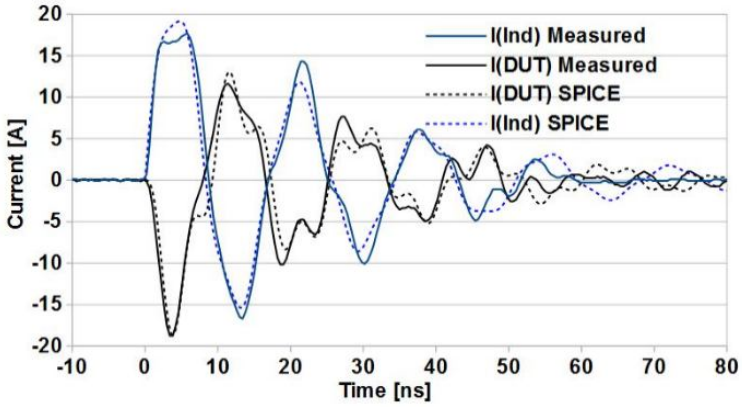

Figure 65. A simulated and measured discharge waveform I_{DUT} with a field-collapse event test method.

Basically, discharge current waveforms are the most accurate parameters for control purposes, but fast ESD events are challenging to measure exactly in manufacturing. Instead, quasi-static potential and the charge of ESDSs can be monitored by using basic handheld tools [a][c]. These two values can be extracted from a DUT stress test when the discharge environments are similar both in a test bench and real process. It is still important to document all the test setup and stress level parameters. For example, compared to a standard HBM, the source parameters are not fixed in a real life CDM, CBE, CDE, or FCE testing. The stress level depends on the size of the DUT and dimensions of the test setup. Therefore, the stress levels should not be expressed in terms of only voltage without any additional information. Other essential parameters are the peak current (if available), source capacitance, charge transferred, and potential energy. In addition, resistance and inductance of the discharge event should also be provided when available. It is also recommended to include current waveforms and an integrated charge transfer in the test report.

ANSI/ESD S20.20-2014 has a 200 V CDM limit and maximum 35 V limit for floating conductors [14]. However, based on observations with ESD failure cases and subassembly level sensitivity tests, these limits are not realistic in the electronics assembly environment. The 200 V limit is targeted for single ICs not commonly handled in electronics assembly. The 35 V limit is linked to an ionizer ion-balance target, but most subassemblies will not fail with the 35 V level; instead, the real voltage sensitivity depends also on the source capacitance, peak current, length of the pulse, and total charge of the ESD event. Trying to keep all floating conductors, such as electro-mechanic parts, below 35 V would lead to excess use of ionization and extra costs with ESD protection. In addition, most subassemblies have failed in a process and test bench when the source potential has been over 500 V and stored charge has been more than 10 nC. Naturally, this depends on the type of the electronics and at which contact point on the ESDS the discharge is made.

An example control table for assembly operations based on the potential and charge values is presented in Table 5. There are two different sets of limits for two product families with varying ESD sensitivity, and these values apply both to ESDS and the mechanical parts used in the process area. ESD-based failures can be prevented by keeping ESDS and mechanic part charges below these limits.

Table 5. An example warning and alarm levels for ESDS charging for two different products.

	Product 1		Product 2	
Action	Charge	Potential	Charge	Potential
	[nC]	[V]	[nC]	[V]
Do corrective actions	> 10	> 400	> 30	> 1000
Warning limits	5 - 10	200 - 400	10 - 30	500 - 1000
Safe level	< 5	< 200	< 10	< 500

6.5 Corrective Actions in the Process Area

ESD risks should be analyzed for each new electronic product or process phase coming to the assembly area. Here, the EMI signals, charges, and potentials are measured as part of the compliance verification process. If the measured maximum charge and potential values are below the set alarm limits, no corrective actions would be required. In addition, as long as either of the values stay below the corrective action level, no ESD failures should occur. However, the warning level is a grey zone, and ESD risk prevention activities should be undertaken if they are simple to deploy and economically justified. The corrective action limit is the level where some of the ESDS parts have failed during stress tests; therefore, corrective actions have to be taken.

The risks can be controlled by preventing the ESD/EMI event or by decreasing the stress level of the event. A common preventive action is to remove the physical metal-to-metal contact, but this is not always possible when electrical subassemblies are tested or joined together. Therefore, another way is to decrease the amount of static charges with assemblies and thereby limit the stress level.

Corrective actions can be divided into two categories: passive and active methods. An active ESD or EMI preventive action requires that the process or product is controlled in a specific way to prevent ESD or EMI. The active method may require us to install ionizers, ask a worker to do a specific manual operation before an assembly, or redesign the product to make it more robust. A common challenge with the active preventive methods is that they depend on the process stability and functionality. In addition, the active method typically increases cost of ESD protection.

Adding ionizers is often an effective way to prevent ESD risks, but the level of protection depends on the operation of the ionizer; thus, the tool must be periodically monitored. One common source of ESD failures has been a broken ionizer. The ionizers have also an important role with contamination control. A high-pressure ionized air stream can remove contaminants from surfaces and decrease the effect of electrostatic attraction [118]. The ionization requires time to neutralize static charges on surfaces. Here, the main challenge is with charged small-size objects that are moving, such as single ICs in a placement process. Those can require more than 5 s to get fully neutralized by ionization. In addition, in a large FA, the area can have thousands of process phases where ionizers could be placed. This has led to overkill with the usage of ionization, and there are large-size factories with more than 10,000 ionizers installed with 5–10 M€ investment and running costs measured in 1–2 M€ in a year [119].

In a passive method, the environment, the product, or material selection is tailored so that the risk is mitigated without major investments. Passive methods are typically more desired, as those can be faster and more affordable to deploy. Common passive protective methods are to prevent ESD events with a dissipative contact material or to change the dynamic capacitance of the ESDS when there is metal-to-metal contact. For example, a charged plastic cover with electro-mechanic components can be placed directly on the surface or close to a conductive surface and not on a dissipative plastic assembly support. This can multiply the dynamic capacitance of the cover, thus decreasing the quasi-static voltage of the part during the assembly phase based on equation (1). This will also limit the energy content of the ESD event based on equation (2). Naturally, this method requires that the cover is charged in a low capacitance environment. ESD risks can also be avoided by changing the order of process handling. For example, changing a first-in-first-out buffer to first-in-last-out buffer gives time for static charges to dissipate; thus, there is no need to add additional protection tools in the process. More examples of different correction actions can be found, for example, in the references [c][d][2][40][49][51][57][59][94][109][111]–[113].

7 Discussions

ESD and EMI control methods presented in this thesis were deployed in more than 10 large-size electronics assembly facilities at NOKIA Corporation. ESD control programs were built separately in each facility and tailored based on the type of the products and processes. All these programs were based on the ANSI S20.20 and IEC 61340-5-1 standards but had additional process and product specific layers, as presented in Figure 56. All the facilities were audited periodically and guided to deploy the best practices in parallel. The facilities were also informed of the ESD sensitivity of subassemblies with a generic warning and alarm limits based on potential, charge, and EMI pulse amplitude information. The sensitivity information was generated in an electrostatics test laboratory and R&D facilities. The potential, charge, and EMI parameters in EPAs were controlled by the local ESD responsible. However, most ESD teams did not measure discharge waveforms, and they had not detailed HBM or CDM component level ESD withstand information available.

Before implementing the additional control methods, there were several major ESD and disturbance cases found in each year. Not all of them were related to product failures but also on yield problems decreasing manufacturing output when ESD or EMC problems in a specific process phase halted the whole process throughput. This has led to higher losses than replacing or reworking failed products. When the additional control methods were deployed in the facilities, the level of major ESD and EMI failures decreased to close to zero. There were actually four years in a row without a single major ESD or EMI failure or disturbance cases found (hundreds of millions of different products were made during the period). After four years, there was a major failure case when an ionizer broke in an automated process equipment and *light emitting diode* (LED) components started to break on a flex PCB due to a CBE discharge.

When the challenge of ESD and EMC issues was more or less solved, the main focus was shifted to decrease costs of preventive methods. Here, the corrective principles discussed in the Chapter 6.5 were deployed, which brought significant yearly savings measured in millions of euros. A major part of the savings came from optimized package materials where dissipative or electrostatic discharge shielding type of packages were replaced with dielectric materials. Here, an effective electrostatics test laboratory with a competent team was a vital part of the operation.

The main challenges with the advanced control methods were related to achieve and maintain competences of the ESD responsible. ESD team members are not always familiar with electronics, EMC, RF, and material technologies and even less with electrostatics and ESD phenomena. One additional challenge comes when the ESD team must be able to control all materials and processes in the facility over the organization boundaries. It requires a few years to obtain a solid competence to analyze assembly processes with different electrical measurement methods, to become familiar with the process phases, and to make correct decisions to implement efficient corrective actions. Therefore, a new ESD team should acquire training services and cooperate with organizations, such as with the EOS/ESD Association, to obtain competences to make efficient decisions.

On top of the facility control, it is not so straightforward to carry out product ESD sensitivity analysis on a subassembly level. System designers typically do not know where and how the products will be assembled. They are neither able to provide much data about the ESD sensitivity of subassemblies, as those are not always tested individually or designed in-house. Therefore, subassembly level testing must be done by the facility ESD responsible or, preferably, by a test lab with the knowledge of the used assembly processes and the product itself. The assemblies can be also highly valuable, and extra ESD tests are not possible. In that case, it is more straightforward to deploy all available preventive methods in the process area.

8 Conclusions

The novelty of this thesis is to first time combine IC level ESD qualification information, system level ESD/EMC design information, assembly process, control measurement methods, and statistical information of the found ESD failure and disturbance cases to optimize ESD control methods in electronics assembly. It is show that current ESD control methods in electronics manufacturing have major deficiencies to detect and control ESD failures and disturbance cases. It is also shown that HBM and CDM qualification information alone cannot be used to assess ESD risks, and therefore, the common approach to ensure ESD safe handling of electronics based on the measured voltage levels can lead to overprotection, excess costs, and false sense of security.

Based on the analysis in this thesis, electronics assembly areas fulfilling the current IEC61340-5-1-2007 and ANSI S20.20-2014 standards can effectively prevent ESD failures, which are related to manual handling of ESDS. In addition, there are only few ESD-related challenges in an assembly with single IC components, as those are handled inside controlled automated handlers, and the ICs are packed in protective materials during logistic phases. However, less attention has been paid on ESD risks, where product parts are charging and discharging into other product mechanics or into electrical ground. In addition, prevention of cable discharge events is not always part of the ESD control program. Additional challenges exist with electrical process equipment being sensitive to electromagnetic disturbances, which causes system failures and decreases production throughput.

As a conclusion, to improve current ESD control programs in the electronics assembly, additional control methods would be needed. Here, the focus should be with final assembly and testing process phases where about 90% observed failure and disturbance cases have occurred. Of these events, CDM, CBE, and CDE discharge events cover about 60 % and equipment or product disturbance cases about 30 %. When these failure events are compared with the failed component HBM and CDM withstand voltage data, no correlation can be found. This can be explained with different discharge scenarios found on a subassembly level than used in a HBM and CDM qualification. In addition, the HBM and CDM voltage is reported based on the most sensitive I/O, but discharges in the assembly area may not go through the sensitive I/Os. Therefore, it is challenging to justify or build ESD control methods in electronics assembly processes based on component HBM and CDM withstand voltage information.

Most failed ICs on a subassembly level occurred on those ICs having several external connections to on-board test pads and connectors. These connections can be easily accessible and may not have designed extra EMC or ESD filtering in place if the contact point is well protected in a final complete system. In addition, the on-chip protection can only be designed to provide protection at limited level, and, on a subassembly level, the discharge waveform can exceed typical HBM or CDM qualification stress levels due to a higher discharge source capacitance and different current paths along the PCB.

In an improved ESD control program, EMI control, a product part and cable charge control are added into the program, together with groundings and other basic controlled EPA items. Charging of product parts is monitored with potential, discharge current, and charge meters, and that data is used together with process analysis to detect known ESD risk scenarios, i.e., HBM, CDM, HMM, CBE, and CDE. Electromagnetic pulses should be measured with an oscilloscope and antenna or detected with radio receivers. These tools are the same as those used to locate possible ESD events in EPAs. However, to measure and control these additional ESD and EMI risks require us to use nonstandardized tailored risk analysis, measurement tools, and control methods; also, broader ESD responsible personnel training and competences are needed.

This dissertation shows that ESD and EMI events leading to product failures or disturbances in the electronics assembly are typically random in nature, and detection of the risks requires statistical approach. The risks can be analyzed and detected, for example, with DFMEA methods. With these, the realized risk level can be quantified based on a failure severity or consequence of the failures, and this information can be used to focus preventive actions on the most severe process phases. This will limit required investments on ESD control.

One part of the risk analysis is to understand the real ESD sensitivity of the products in the process. Unfortunately, there are no standardized methods available to test subassembly level ESD immunity. In this thesis, it is proposed to use CBE, FCE, and CDE methods, which simulate the real world ESD scenarios found in the process area. With CBE, CDM, and CDE the discharge waveform is device dependent and simulates a discharge scenario where the ESD waveform is a step response of the circuit when the charged object is grounded. These methods can provide several stress parameters for a practical risk assessment in the assembly area, such as a maximum potential, charge, peak current, and energy the DUT survives. Of these parameters, the potential and charge values are proposed as the primary control parameters. The potential and charge can be measured in a process area with portable meters with reasonable accuracy. In addition, these quasi-static measurements are easier and much faster to build than discharge current analysis.

For EMI control, portable detectors are proposed as the primary tool. These can detect possible ESD events in the process area. More accurate information can be generated with an oscilloscope, contact probes, and antennas, which provides amplitude, frequency data of the events, and also the exact location of the EMI source with multiple antennas and software tools. Oscilloscopes with calibrated antennas can be used to define warning and alarm limits for the maximum disturbance levels close to sensitive process phases. However, oscilloscopes require more competence from the ESD responsible, and these tools are not currently commonly available in all electronics assembly areas. There also can be several major continuous EMI sources from electrical motors, power sources, and HV systems that will hide EMI signals from ESD events.

Finally, with the additional control methods presented in this thesis, more than 10 large electronics assembly facilities got close to zero ESD/EMC failure levels. The ESD responsible established an EPA, analyzed assembly processes, measured product part charges, voltages, EMI, and made corrective actions based on the measured subassembly-level sensitivity information generated on test benches simulating the real process environment. At the same time, the ESD responsible had no detailed knowledge of the component level HBM or CDM withstand voltage information. The main challenge with these additional control methods was with the competences. It took, in most cases, two to three years to obtain an adequate competence for the local ESD team to effectively carry out process analysis and corrective actions. There were also challenges to conduct enough subassembly-level sensitivity tests, but this was mostly covered with the collected knowledge of the past designs and ESD sensitivities found with those products. In addition, product ESD sensitivity tests required to build up test benches and required well-trained persons to obtain correct results. An electrostatic laboratory was an essential support in these process and material development phases.

As a final remark, product and process specific ESD/EMC risk should be emphasized in ESD control related standards, standard practices, and technical reports. As a further work, IEC and ANSI/ESD standard committees should include guidelines and methods to assess these additional ESD and EMC risks found in electronics assembly processes. HBM and CDM qualification tests should be further developed to better inform practical data for the product designers and facility ESD team to build up more robust electronics systems and effective ESD control programs. Here, charge and energy limits or TLP IV data could be considered instead of the HBM voltage, and discharge current waveform instead of the CDM qualification voltage information. For that purpose, this thesis gives new arguments and proposes effective methods to implement the required protection based on the real sensitivity level of the ESDS for the future more sensitive electronics devices.

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ESD qualification data used as the basis for building electrostatic discharge protected areas

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ABSTRACT

ESD control programs that are based on the standards IEC61340-5-1 and ANSI/ESD S20.20 are targeted to provide safer handling of electronic parts now susceptible to damage by electrostatic discharge. However, ESD failures have occurred in EPA even when all standard control methods are met. To further improve EPAs, ESD control programs should be updated to cover all known common discharge scenarios, and multiple parallel ESD source parameters should be used to assess the level of ESD risks. In addition, a reliable ESD risk assessment should be based on discharge source circuit analysis and product sensitivity tests using the real discharge waveforms found in EPA.

1.0. Introduction

The electronics industry uses *IEC61340-5-1-2007* and *ANSI/ESD S20.20-2014* standards to build electrostatic discharge protected areas (EPA) [1,2]. These standards are based on the EN100015-Protection of Electrostatic Sensitive Devices, MIL-STD-1686-Electrostatic Discharge Control Program, and the *MIL-HDBK-263 – Electrostatic Discharge Control Handbook*, which are the direct predecessors of the current standards [3]. The basic target of the two standards is to guide industry to define an ESD control program that minimizes electrostatic discharge-based damage. There are additional guideline documents, technical reports, best practices, and standard test methods available that add information on the technical requirements of materials and how to implement, maintain, and control EPA.

The IEC61340-5-1-2007 and *ANSI S20.20-2014* standards have been updated over the past three decades, but the basic assumptions have stayed the same. One of these is to use a *Human Body Model* (HBM) 100 V limit as the base for building an EPA and ESD control program [1,2,4]. *ANSI/ESD S20.20-2014* offers an additional 200 V *Charged Device Model* (CDM) and 35 V on isolated conductor target values [2]. Most of the technical requirements, such as shoe-flooring combination resistance or wrist trap properties, are based on the same target value, which is to limit person charging below 100 V. However, the HBM and CDM qualification standards state that these should be used only to compare electronic component ESD robustness between different suppliers [4–6].

The component HBM, CDM and *Machine Model* (MM) withstand voltages have been compared to ESD risks and field failure levels in several publications, including white papers from the *Industry Council on ESD Target Levels* [3,8–10,12,14,15]. Additional discharge events found, such as the *Cable Discharge Event* (CDE) and *Charged Board Event* (CBE), have been studied in several papers [9,11–16]. These papers indicate ESD failure cases in EPA even when the basic 100 V HBM target is fully met. Therefore, it is wise to ask if the definition to establish EPA, as based on 100 V HBM, 200 V CDM and 35 V on isolated conductor targets, is accurate, adequate and comprehensive enough. In addition, when the 100 V HBM is used as the main target, why are there still destructive ESD events in EPA and what additional scenarios and targets should the ESD control programs further include? These questions further relates to changes in electronics manufacturing wherein automation has mostly replaced manual handling of single components and major part of final assembly phases.

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In order to understand 100 V HBM stress level, in Section 2 we first analyse HBM discharges in a HBM tester environment and in a real world EPA environment. Here discharges from a person and then *Human Metal Model* (HMM) pulses are analysed in more detail. CDM and CBE/CDE types of discharges in an EPA environment are presented in Section 3. Based on these results, additional EPA control methods are proposed in Section 4. Finally, Section 5 summarizes the results.

2.0. HBM discharges

The HBM withstand voltage may not necessarily relate to the level of sensitivity of electrical components in a real life situation, but more or less this information is used with EPA targets. Therefore, the HBM current waveform and the stress level it produces are studied in further detail.

2.1. The HBM discharge waveform in a tester environment

The HBM discharge source circuit has a 1500 Ω serial resistor and a 100 pF source capacitance. The discharge is given to one pin at a time, while another pin, or a group of pins, is grounded to an electrical ground. The standard also defines the current waveform details with a pulse rise time, peak current, decay and maximum ringing current values for both a short and a 500 Ω load [4]. The details are available for a short load between 125 V and 8 kV. For the 500 Ω load, only the 1 kV and 4 kV points are given [4,3]. The lowest voltage level with given parameters for a short load is 125 V; however, typical maximum and minimum current values are also calculated for 100 V, where the calculated minimum peak current is 60 mA and the maximum peak current is 73 mA. The rise time for the peak current can vary between 2 ns and 10 ns, while the pulse decay time can vary between 130 ns and 170 ns. The minimum and maximum discharge peak current values can vary ± 10%; however, in practice, the peak current depends on the known 1.5 kΩ source and an unknown *Device Under Test* (DUT) internal resistance.

The standard ANSI/ESDA/JEDEC JS-001-2011 has not specific value for the parasitic inductance *L*, which is a combination of tester parasitics and DUT parasitics. The boundary values can be extracted by searching the values that fulfil the minimum and maximum HBM pulse rise time requirements with a fixed 100 pF source capacitance. The initial part of the simulated standard HBM waveforms are presented in Fig. 1 with L_{min} = 640 nH and L_{max} = 4700 nH, which gives 2 ns and 10 ns pulse rise times for a short load. With a 500 Ω load, the inductance values can vary even more, and the peak current values decrease. The initial part of the HBM pulse will vary based on the inductance, and the pulse can create different ESD failures, depending on the turn-on speed of the DUT ESD protection [3]. The real world HBM discharge can have a much faster rise time, and with over 1 kV discharges, the rise time will vary between 50 ps and a few nanoseconds [17,18]. Humidity and the geometry of the physical discharge event also affect the realized HBM current waveform. One example of the real world HBM waveform is presented in Fig. 1, using the analyses of Viheriäkoski [19] and Barth [17,18]. However, in a component tester, the rise time is slowed on purpose to meet the standard specification, and the rise time can be more than ten times slower than the reported real world values.

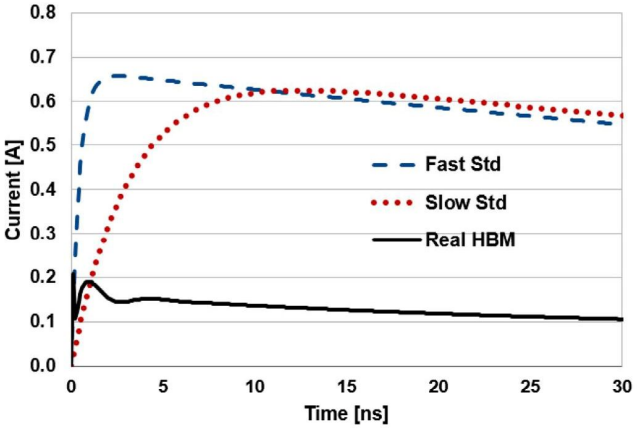

Fig. 1. The figure shows the 1 kV HBM discharge currents with maximum (t_r = 10 ns) and minimum (t_r = 2 ns) rise time based on the ANSI/ESDA/JEDEC JS-001-2011 standard. A measured 1 kV real life HBM discharge for comparison.

The realised HBM stress level in a HBM testing environment is calculated in Table 1 for under-damped pulses between 50 V and 800 V (excluding DUT intrinsic *RLC* and air spark parameters which also vary). These parameters are close to the worst case values with HBM at low inductance and total energy content, and will be compared later to estimate how well HBM represents other typical discharges found in EPA. The maximum current rise time rate *dI/dt* is based on the derivative calculation *Lim* (di/dt) when t→0. It is also good to point out that in a HBM stress only part of the pulse energy burns in the DUT. All the current is forced through the DUT, while the 1500 Ω serial resistor limits the voltage over DUT and limits the energy and power stress levels as well, depending on the resistance of the device. For example, if the DUT has 30 Ω resistance during 100 V HBM pulsing, only 2 V (2%) of the voltage is over the DUT, and only 0.13 W (2%) of the power heats the device.

Component ESD robustness against HBM discharge is reported by using the maximum discharge voltage the DUT survived [4–7]. Sometimes the most sensitive pin combination data is also available, but this data is not visible on most component data sheets. In addition, not all pin combinations are tested in order to decrease testing time and prevent excessive ESD stress [3,4]. What is also missing from the data sheets is the exact failure current, the rise time of the pulse, and the failure type with its reported voltage level. The maximum safe discharge charge *Q* (*nC*) can be calculated based on the known voltage and 100 pF source capacitance, but that charge can be irrelevant without the exact current and time (*It2*) failure information. Transmission Line Pulses (TLP) offers one more test method that can be used to simulate HBM stress and provide more detailed IV-curve data about the DUT sensitivity. However, the TLP methods are not yet accepted for DUT qualification purposes [20]. In summary, the HMB withstand voltage provides only limited information about the real ESD sensitivity of the DUT.

2.2. Real world HBM discharges in EPA

In 1991, Bailey et al. [21] presented a paper wherein the person capacitance varies between 60 pF and 170 pF, and the HBM discharge current from a finger has a rise time from a few

Table 1
Short circuit HBM discharge parameters with *RLC* values of 1500 Ω, 1000 nH and 100 pF.

Voltage	Rise time	Peak current	Charge	Energy	Peak power	Max dI/dt
[V]	[ns]	[mA]	[nC]	[μJ]	[W]	[A/ns]
50	2.8	33	5	0.13	1.6	0.05
100	2.8	65	10	0.5	6.4	0.1
200	2.8	130	20	2	26	0.2
400	2.8	260	40	8	103	0.4
800	2.8	520	80	32	410	0.8

nanoseconds up to microseconds with 200 V discharge potential. When a person had a metal tool in hand, the initial peak current increased up to 700 mA, and rise time was about 1–2 ns with 200 V. However, that measurement was limited by the measurement set-up and faster and higher peak currents were estimated to be possible. Taka et al. [22] measured and simulated HBM discharges with 600 V by using fast oscilloscopes. They also observed that the discharge peak current from the fingertip decreases down to 40 mA and is significantly less than the values in standards with a 600 V potential level. With Human Metal Model (HMM) pulse, the rise time was around 100 ps, and the peak currents could go up to 3 A.

Similar results were presented by the authors in a paper *Low Level HBM ESD* [19]. The HBM tester set-up and the real world discharge parameters are compared in Fig. 2a. The resistance depends on the discharge voltage and only with over 2000 V potentials is the resistance close to the standard 1500 Ω. Below 500 V, the human body resistance is significantly higher than that of the standard values. The effect of high resistance can be seen in Fig. 2b where the discharge peak current is compared for a HBM tester and a real world HBM event. The real world discharge has a peak current of about 0.6 mA and is about 100 times lower than a typical HBM stress with 100 V in a tester. This paper also presents HMM discharges with 100 V. The results closely support Bailey's observations, and the HMM peak current is about seven times higher at 550 mA than with a bare finger discharge. The pulse rise time and decay time is also faster, and the resistance is lower than 1500 Ω when the discharge comes from a metal object. However, object size, discharge geometry, relative humidity, and *RLC* parameters will affect the HMM pulse.

Barth et al. [17,18] in their papers indicated that the initial part of the real world HBM discharge can have a very fast rise time and varying discharge resistances. A humidity dependent air spark resistance and the shape of the electric field in the discharge point affect the HBM waveform. Higher humidity and sharp shape discharge points can slow down and attenuate the pulse. The authors also showed that an actual HBM current waveform can be modelled more in detail by using three parallel exponential decay regions that are different from the standard decaying HBM waveform.

It is worthwhile to mention as well that it is hard to initiate discharges from a human finger when the potential levels are around or below ~500 V. Under 100 V, weak and random real life HBM discharges are also hard to measure precisely, as the current is typically below 1 mA [19]. However, in a HBM tester, it is possible to create and measure HBM discharges very accurately down to around 10 V and a 6 mA level.

The real world HBM discharge also depends on dynamic discharge source capacitance. In Fig. 3, two discharges from a person's finger are shown with the same initial 950 V potential.

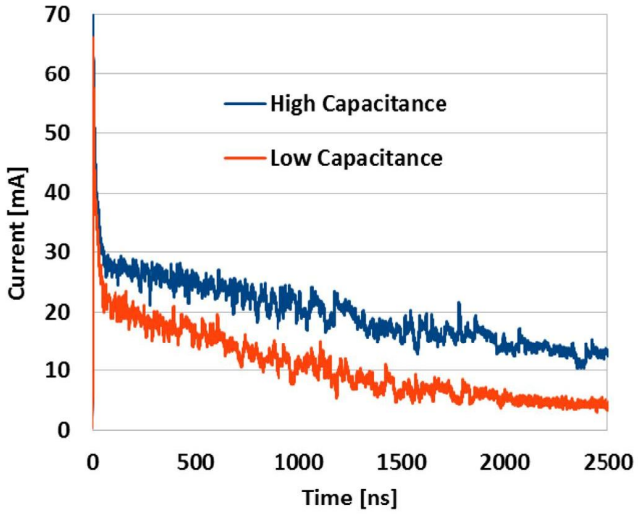

Fig. 3. HBM discharges from a person standing on dissipative mat with high and low dynamic capacitance. The quasi-static source capacitance is 100 pF and the initial potential is 950 V.

Repeating HBM pulses at a 950 V level is still poor, and the presented waveforms are just averages of 16 pulses in a 40% RH. The person wears dielectric shoes and stands on a grounded dissipative mat on top of a wooden floor and secondarily on a dissipative mat with a grounded metal plate under the mat. In both cases, the measured quasi-static capacitance of the person is 100 pF. The varying parameter here is the dynamic capacitance C_{ESD} during the discharge event [13]. The dynamic capacitance is higher on a dissipative mat and metal flooring, so we see a higher discharge current and charge transfer with the same initial potential. In addition, combination resistance or body potential measurements in a walking test cannot reveal the difference, as both are quasi static measurements. Fast discharge measurements are required to reveal that different HBM scenarios are possible with the same voltage and quasi-static source capacitance.

2.3. HMM discharges between two conductive objects

A common scenario in EPA is when a person or equipment joins components, cables, or sub-assemblies to another sub-assembly/mechanics that are stationery on the assembly stand. In such a phase, a discharge between two conductive objects can be more severe than a bare human body discharge event and can be modelled as a HMM, CDE, or CBE discharge. The event can also have

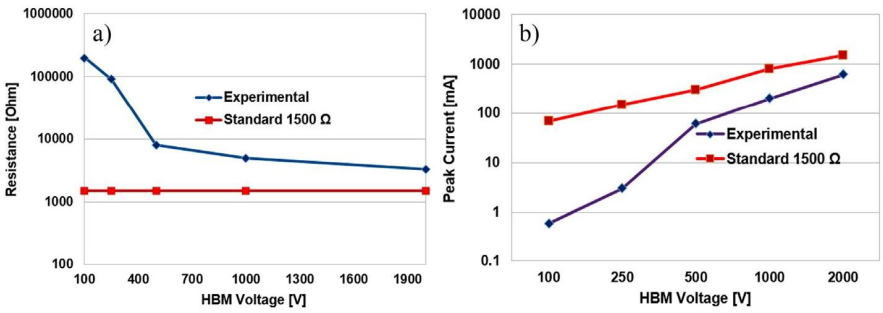

Fig. 2. Left a) Resistance of the HBM in a standard test set-up and in a real world discharge event. Right b) Peak currents in the standard test set-up and in a real world discharge event.

one or two main phases, depending on the scenario, and the initial fast part of the event is similar to a CDM between two conductive objects. The following slower part of the pulse can be from the charged person or other source capacitance, and will flow through the component into the electrical ground or another conductive object.

It is common to find static potentials on sub-assemblies up to a few kilo-volts in EPA when sub-assemblies have dielectric materials [13,14]. Naturally, this circumstance depends on the relative humidity, handling methods, and whether it is possible to use ionisation to neutralise charges in the processing area. The challenge with such a discharge scenario is that normal EPA control methods based on personnel and equipment grounding may not be effective, as demonstrated here with HMM discharges between products kept in hand and a non-grounded conductive metal plate.

The product used in this study is an assembled multilayer PCB with a size of 130 × 55 mm and a metal plate with the same size to simulate product mechanics. A person stands on a dielectric surface holding the PCB in hand, so that the total capacitance of the person-PCB combination is 120 pF. At first, the person-PCB combination is charged up to 100 V; then next, the neutral non-grounded metal plate on the assembly stand is touched with the ground layer of the PCB. In the second discharge scenario, the same set-up is used, but now the metal plate is charged to an opposite −100 V potential and is grounded by the person-PCB combination with zero potential. The test circuit and the measured discharge current *IESD* during the first 20 ns period are both shown in Fig. 4. As expected, the same current waveform and charge transfer occurs in both discharge events, and the strong initial part of the discharge hides the HBM current waveform. Thus, it is not enough to control personnel and equipment groundings alone, as about the same discharge event can occur when mechanics, PCBs or other conductive objects in EPA have static charges and discharges into other objects. HMM events can also produce significantly stronger discharge events than HBM events with the same initial voltage difference due to the metal-to-metal contact.

3.0. CDM, CBE and CDE discharges in EPA

3.1. CDM events in EPA

CDM sensitivity of IC devices can be tested, for example, according to the standards JESD22-C101 or ESD-STM S5.3.1 [5,6]. The CDM standards define a test method that is reproducible between different test labs – but their purpose is not to represent any specific real life ESD scenario in EPA. The CDM discharge is very fast having a pulse rise time around 100 ps. The peak current will vary depending on the DUT, and the total length of the pulse is typically a few nanoseconds [9]. The event simulates a case where a charged device is grounded by touching one of the leads with a low inductive contact. Therefore, the CDM pulse is faster than HBM, and thereby, DUT failure mechanisms can be different. These failures can be related to the excess E-field through dielectrics, such as CMOS oxide layers or the peak power of the pulse. Similar failure mechanisms to those produced by the CDM testing have also been found in manufacturing fulfilling EPA requirements [9,13,14].

CDM discharges can occur in EPA, for example, when a charged IC device touches a metallic surface, or when a charged IC device is touched with a pogo pin in a tester. When components are soldered onto a PCB, the CDM events are no longer similar, as the board will change the discharge event [8,14]. Therefore, CDM is a more realistic scenario in a wafer manufacturing, back-end processing and tape and reel packaging where wafers and single ICs are handled by several process steps. CDM discharge parameters that are based on the selected *RLC* parameters are presented in *White Paper 2* [10] and calculated also in Table 2 with 35 Ω serial resistance. When the calculated values are compared to those in Table 1, it is evident that the CDM events have very little common with HBM discharges. CDM control also requires different control methods than HBM as the main source oft he charges is the product itself.

In a surface mount assembly process, single IC devices are not handled manually due to designed automated assembly phases. ICs are typically not touched by the operators due to an increased contamination risk, and for example, in the rework phase, operators use vacuum pick-up tools or tweezers to handle single components. Therefore, component placement process is the only phase during the electronics assembly where a single IC touches another surface, a highly resistive solder paste. These processes are typically kept well under control, and very few CDM ESD failures have been presented in publications when compared to the huge amount of IC components actually assembled. The rest of the manufacturing phases in an electronics assembly contain more or less only assembled PCBs and sub-assemblies, and thus, CDM events similar to the CDM tester environment are hard to reproduce.

The reported CDM withstand voltage alone is a pretty hazy value to use to estimate ESD risks [5,6,8,10]. The voltage is the maximum level IC devices that survived in a tester, but the reported voltage is not the same voltage level as that used in a CDM tester during the stress test. The voltage in a tester is adjusted based on the CDM discharge peak current target during the tester calibration phase. Different CDM standards also stress the device at different

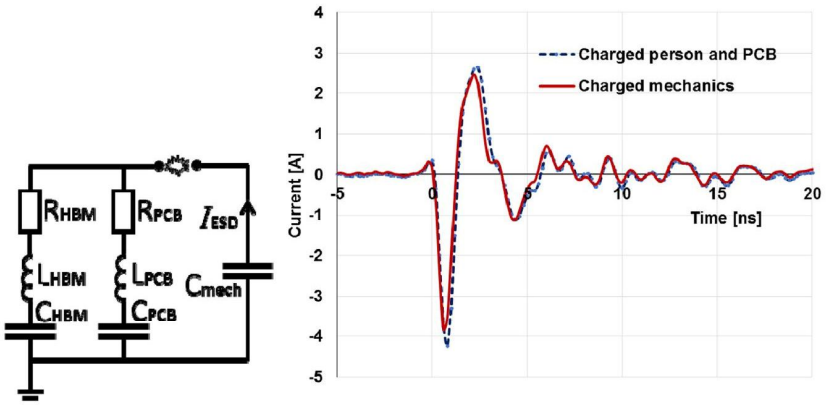

Fig. 4. The test circuit and the measured discharge current I_{ESD} waveforms.

Table 2
Calculated CDM discharge parameters with the following *RLC* values: 35 Ω, 5 nH and 2 pF.

Voltage	Rise time	Peak current	Charge	Energy	Peak power	Max dI/dt
[V]	[ps]	[A]	[nC]	[μJ]	[W]	[A/ns]
50	100	0.64	0.1	3	14	10
100	100	1.27	0.2	10	57	20
200	100	2.5	0.4	40	225	40
400	100	5	0.8	160	900	80
800	100	10	1.6	640	3600	160

current levels with the same reported voltage. The IC device itself also causes a lot of variation in the realised CDM stress level, as the capacitance of the component in a tester is not taken into account when the withstand voltage is reported. The CDM tester environment represents a typical worst case discharge scenario, one not easily found in real life scenarios [25,26]. From this point of view, it is thus possible to estimate that an IC device should survive a discharge at least with the reported CDM voltage in EPA. However, in the real life this relationship has uncertainties and can lead to both underestimation and overkill with ESD protection methods in EPA [9,13,14,25].

3.2. CBE and CDE events in EPA

CBE and CDE are in principle similar to CDM, but there are major differences between the events. In a CBE/CDE, the charged objects are larger than a single IC device; thus, the source capacitance and the inductance of the discharge path can be higher. The extra capacitance increases the peak current, transferred energy, pulse rise time, and power of the event. The extra inductance increases the pulse rise time and together with a small serial resistance, it may create oscillating under-damped waveforms [16]. However, the very first peak and rise time of the current pulse can be similar to CDM in some discharge scenarios. Therefore, CBE/CDE can produce similar ESD failures to those for CDM, but also produce failures due to excess energy and power and lead to similar failures as found with electrical overstress (EOS) [9,11,13–15].

CBE/CDE scenarios are common in assembly and field operations due to their system/module level process phases. A typical CBE/CDE event initiates from the charged insulators used in the product itself. The insulator can be a cable insulating material, a display panel, a plastic cover used to encapsulate a PCB, or even the PCB itself. In addition, induction by electric fields can induce charges on isolated conductors and cause CBE/CDE risks. Here the 35 V limit on isolated conductors based on *ANSI/ESD S20.20-2014* can be challenging to deploy on product parts. These parts may contain both dielectric and conductive materials and typically have some amount of electrostatic charges that exceed the 35 V limit. Trying to keep these parts below 35 V may also significantly increase the cost of ESD control without a comparable benefit.

The typical CBE discharge *RLC* parameters are presented in Table 3 for the calculated discharges shown in Fig. 5 with 100 V initial potential. These example waveforms are copied from real world cases measured in an EPA environment. In Table 3 the waveform *A* has a low discharge resistance and oscillates due to the high inductance. Waveform *B* has two parallel oscillating pulses together wherein the high frequency component attenuates away within the first 30 ns. This waveform *B* is typical in CBE/CDE where the fast pulse originates from the metal-to-metal contact, and the slow part of the waveform is set by the board/cable dimensions. Waveform *C* oscillates, but the spark channel closes after 45 ns. However, the discharge may start once again after a short period. Waveform *D* is a discharge from a high impedance I/O on board and Waveform *E* is a discharge between a small antenna and an electrical system. It is also good to point out that these waveforms are just examples to illustrate the variety of CBE/CDE. In addition, these waveforms can be even faster in a real life, as the measurement set-up always adds resistance and inductance to the discharge path. Therefore, the pulse rise time, peak current, power and max *di/dt* values can be faster or higher than the presented values.

3.3. A comparison of different discharge events

The typical discharge parameters for the five scenarios discussed here are presented in Table 4 with a 100 V initial charge level. CDM can damage electronics due to high peak current, current rise time and power levels, even when the total transferred energy content is low. HMM events have an even higher charge transfer and peak current levels, whereas HBM events are the weakest. CBE and CDE can have significantly higher stress levels except with a current rise time which is the fastest with CDM events. CDM/CBE/CDE are also realistic ESD scenarios in EPA and due to high stress levels these may damage electronics. In addition, real life HBM and CDM events have highly varying rise times, peak currents, source capacitance, power, and energy content. Similarly, CBE/CDE/HMM events will vary depending on the environment and on the electrical parameters of the objects taking part in the ESD event.

Applying Table 4, any safe potential limit is hard to give for any of these discharge scenarios, as the product itself and the close environment defines the stress level; thus, several discharge parameters are required to define the severity of an ESD event fully. An exact risk estimation would require product sensitivity tests with the real world discharge waveforms found in the handling process and should be undertaken in a controlled laboratory environment. At any rate, product sensitivity analysis can still be carried out and used to assess real world process ESD risks as already presented in several papers [8,9,13,23–26].

4.0. Improving ESD control programs

Based on this previous analysis, current ESD control programs are not always able to prevent ESD damages in EPA. On top of actual ESD events, there can be *electromagnetic interference* (EMI) initiated product and equipment disturbances in an EPA environment. This

Table 3
CBE discharges with 100 V initial potential. The discharge waveforms are presented in Fig. 5.

	Capacitance	Inductance	Resistance	Rise time	Peak current	Charge	Energy	Peak power	Max dI/dt
	[pF]	[nH]	[Ohm]	[ns]	[A]	[nC]	[μJ]	[W]	[A/ns]
A	50	150	5	3.6	1.7	5	250	225	0.67
B	100&5	150&50	20&20	0.6	2.2	10.5	520	69	2
C	50	150	15	3.2	1.5	5	250	250	0.67
D	70	43	50	1.4	1.5	7	350	109	2.3
E	5	50	30	0.6	0.8	0.5	21	23	2

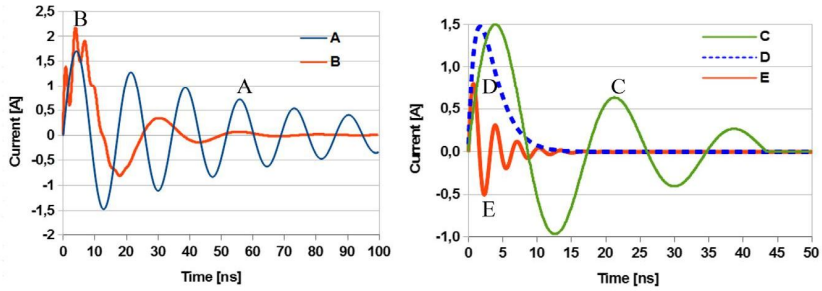

Fig. 5. CBE discharges with a 100 V potential level based on the calculated *RLC* parameters in Table 3.

Table 4
Typical discharge parameters with a 100 V initial charge level.

100 V	Rise time	Peak current	Charge	Energy	Peak power	Max dI/dt
	[ns]	[A]	[nC]	[μJ]	[W]	[A/ns]
HBM[1]	2.8	0.065	10	0.5	6.4	0.1
CDM[2]	<0.1	1.27	0.2	0.01	57	<20
HMM[3]	0.2–3	<5	<10	0.5	<20	<15
CBE[4]	0.3–3	<15	<300	<1.5	<700	<15
CDE[4]	0.3–3	<15	<300	<1.5	<700	<15

Note: [1] from Table 1, [2] from Table 2, [3] with 10 Ω serial resistance, [4] with < 40 nH serial inductance.

scenario is the author's experience as seen in electronics manufacturing facilities over the last twelve years, where CDM, CDE, CBE, and EMI events have represented more than 90% of the found ESD/EMI electronics failures and disturbances in EPA [13,29]. ESD control programs and standards should be improved to contain these additional challenges, and those additional control methods are proposed in this section.

4.1. Extended coverage of ESD control programs

An improved coverage of ESD control programs is shown in Fig. 6a where detailed control of product parts is added into these programs, together with groundings and other controlled basic EPA items. The program is based on the existing ESD control methods wherein the main parameters to monitor are the groundings, material conductivity, static *E*-fields, and surface potentials. Charging of product parts in EPA should be monitored with potential, discharge current and charge metres, and that data should be used together with process analysis to detect all known ESD risk scenarios, i.e., HBM, CDM, HMM, CBE and CDE [8,13,14,25,26]. Once again, these values cannot be directly compared to the IC level HBM or CDM qualification data. Instead, alarm and corrective action thresholds should be based on found EMI disturbance events or set based on the real product and equipment immunity tests. These advanced control methods can produce significant cost savings with optimized investments and process control methods [24,27,29].

The additional dynamic ESD and EMI events require additional non-standardised tailored measurement tools and methods and also broader personnel training and competence. On the other hand, there are fewer items to monitor on the electrical events level, when compared, for example, to EPA groundings and material verifications. This is also shown in Fig. 6b where the control program is presented with three layers. The first control layer is the basic EPA built based on the current standards. On top of the EPA there is an additional equipment specific control layer. This will include all process equipment requiring tailored ESD protection methods. The last third layer has the focus with product parts. Here charging and dynamic events during product part handling are the main controlled parameters. The process control requires more competence at equipment and product level, but can focus more on specific ESD risk scenarios.

4.2. Warning and alarm limits based on an analysis of the process

The existing standard guidelines for EPA should be used to define a basic control program. Further, an extended control process will need to define practical and realistic warning and alarm levels for ESD scenarios. For that aspect, the following procedure is proposed:

a. Define the exact warning and alarm limits only for specific ESD risk scenarios wherein normal ESD prevention activities would be challenging or expensive to deploy.

b. Define generic warning and alarm limits for all ESDS parts used in the process based on stress tests that simulate the real

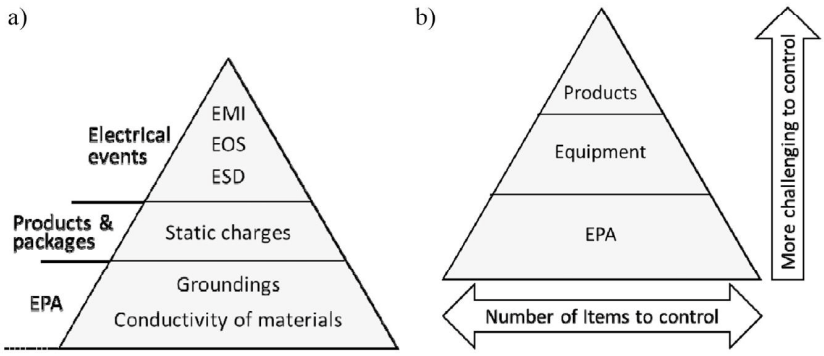

Fig. 6. a) Left – the levels of the ESD control program plan. b) Right – the controlled layers in EPA.

process environment.

c. Use a measured quasi-static charge and potential values with compliance verification measurements to control the CDM, CBE, and CDE risks.

d. Include EMI detection as a part of equipment and product specific ESD risk estimation.

To define the actual realistic limits for the control process, a certain amount of process analysis and ESD stress testing is required. The following procedure is one option that can be used to carry out these tests [11]:

1. Define a critical path for ESDSs and list all those phases where CDM, CDE, or CBE types of scenarios are possible. HBM and HMM events are included, as necessarily.
2. Measure E-field, EMI, charges, and potential levels in each listed phase and select those phases where ESD risks are seen as the most prominent.
3. Define those contact points on each ESDS where ESD events are most likely to occur.
4. Measure discharge environment parameters for each selected scenario in its real handling environment: Capacitance of the ESDS, capacitance of other objects coming in contact with ESDS, resistance of ground paths, etc.
5. Build discharge test set-ups based on the measured environment parameters.
6. Select one to three ESDS parts for stress tests. Stress each ESDS based on its observed potential, charge and E-field levels. It is not necessary to stress all ESDS up to a failure level, as testing can be stopped when the stress level exceeds the maximum levels found in the process area.
7. Define the corrective action limit based on the potential and charge value where the ESDS failed. In addition, define generic warning and safe process limits based on the ESDS stress results.
8. Define the potential and charge limits for the compliance verification. The ESD team will monitor its process capability based on these limits.

Basically, discharge current waveforms are the most accurate parameters for control purposes, but fast ESD events are challenging to measure exactly. Instead, quasi-static potential and the charge of ESDSs can be monitored using basic hand held tools [28]. In addition, these two values can be extracted from an ESDS stress test when the discharge environments are similar in both cases. EMI detection is used in parallel with charge and potential monitoring, as that process offers a way to detect possible ESD events in the area. A control table based on the potential and charge values is presented in Table 5 as an illustration. Here there are two different sets of limits for two product families with varying ESD sensitivity, and these values apply both to ESDS and the mechanical parts used in the process.

Charges and potentials are measured as part of the compliance verification process. If the measured maximum charge and potential values are at a safe level, no corrective actions would be required. In addition, as long as either of the values stayed below the corrective action level, no ESD failures should occur. However, the warning level is a grey zone, and ESD risk prevention activities should be undertaken if they are simple to deploy and economically justified. The corrective action level is that level where some of the ESDS parts have failed during stress tests, and therefore, corrective actions should be taken.

Table 5
Warning and alarm levels for ESDS charging.

Action	Charge	Potential	Charge	Potential
	[nC]	[V]	[nC]	[V]
Do corrective actions	>10	>400	>30	>1000
Warning limits	5–10	200–400	10–30	500–1000
Safe level	<5	<200	<10	<500

5.0. Conclusions

In this paper, both HBM and CDM qualification data and different ESD events were investigated to analyse how to set ESD protection targets for the EPA environment. *IEC61340-5-1* and *ANSI/ESD S20.20* standards define EPA targets based on 100 V HBM and 200 V CDM charging limits and based on the component HBM withstand voltage. The existing technical and control process requirements in these standards have to date been efficient to establish a basic EPA, and thereby, HBM risks are typically kept well under control in electronics manufacturing. However, ESD failures can still occur in those EPAs that are fulfilling the standard requirements.

Discharge events in a component HBM qualification test and in the real world have major differences, and therefore, it is challenging to use HBM withstand voltage information to estimate ESD risks in EPA. Automation in electronics manufacturing has mostly replaced the manual handling of components, and destructive HBM discharges are thereby less likely. The same challenge exists with the CDM qualification data, in which a CDM tester typically produces the worst case results, and the measured voltages in the EPA environment may represent different ESD risk scenarios. In such a case the given CDM withstand voltage should not be used for detailed ESD risk assessments.

There are additional commonly found ESD events in EPA, such as the CBE, HMM, and CDE, which can produce severe ESD damages, often reported as EOS or CDM type of failures. With these events, the same initial discharge potential can damage electronics over a broad range and by using the voltage value alone to assess ESD risk may lead to both over- and under-estimations of the required ESD prevention methods.

To further improve EPAs, ESD control programs should be updated to cover all known common discharge scenarios, and multiple parallel ESD source parameters should be used to assess the level of ESD risks. These additional ESD control procedures should include product part charging, process, and EMI detection analysis. In addition, a reliable ESD risk assessment should be based on discharge source circuit analysis and product sensitivity tests using the real discharge waveforms found in EPA. Here advanced measurement methods, such as product potential, charge, current and EMI detection, will be required. The most detailed ESD risk assessments would be based on the ESD current analysis, but it is also the most challenging control method and indeed requires both sophisticated high frequency tools and solid competence.

6.0. Discussion

Based on the different ESD scenarios, it is challenging to find a solid technical justification for the goal where an EPA built based on these standards is able to prevent all ESD failures with components having ESD to withstand voltages more than 100 V HBM and 200 V CDM. One option would be to remove these fixed voltage threshold values from the standards, and instead, focus on informing how to establish an EPA based on the best known ESD control methods that cover all the different discharge scenarios. ESD control programs could have also different target or detail levels based on the used control methods. This scenario/choice/change would enable simple

ESD protection in those EPAs where the very basic protection level is enough, but also explain the more comprehensive control programs using advanced control principles. To define these required additional control principles would require further work and both standardisation and further measurement method development.

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Correlation of component human body model and charged device model qualification levels with electrical failures in electronics assembly

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ABSTRACT

Electrostatic discharge sensitivity of integrated circuits is compared with electrical failure levels in electronics assembly. Electrical components with a low electrostatic discharge withstand voltage would be expected to have more electrical failures than more robust components. However, the analysis based on 47 products, 14 facilities, and 6 billion integrated circuits show no correlation between electrical failures and electrostatic discharge sensitivity of components. This was found when the withstand voltage of the components is equal or higher than 100 V human body model and 200 V charged device model.

1. Introduction

Electrostatic discharge (ESD) protection in electronics handling based on ESD control programs is established according to the standards IEC61340-5-1 and ANSI/ESD S20.20-2014 [1,2]. A purpose of the program is to establish an electrostatic protected area (EPA) that is able to prevent ESD-sensitive electronics (ESDS) to experience discharges above a 100 V human body model (HBM) and 200 V charged device model (CDM) [3,4]. When more sensitive devices are handled, additional control elements or limits may be required. It is also estimated that ESD sensitivity of components decreases due to the faster data connections and smaller silicon level geometries [5,3,6].

The component HBM and CDM withstand voltages have been compared with ESD risks, field failure levels, and system-level ESD immunity in several publications, including white papers from the Industry Council on ESD target levels [5–12]. The *White Paper I* compared system-level field failure rates to the single component HBM withstand voltages [5]. The data consisted of field failure returns for 21 billion devices with the HBM sensitivity of more than 500 V and shows no correlation between the HBM sensitivity and field returns. A similar study was carried out for the CDM withstand voltage data in the *White Paper II* [6]. This document presents statistics for 9.5 billion components and shows no correlation between field returns and the CDM sensitivity when the CDM withstand voltage is between 100 V and 2 kV.

There is less information available on how the HBM and CDM withstand voltage correlates with a manufacturing failure rate (MFR). The MFR is typically expressed as failing parts per million (*ppm*), and there can be its own *ppm* measures for different failure types, such as the *ppm* for electrical failures. Basically, an EPA should be able to prevent ESD events leading to electrical failures, but ESD failures can still exist in EPA and failure analysis with field returns have revealed EOS/ESD damaged components [7–13]. In addition, electrical components with a low HBM and CDM withstand voltage would be expected to have, in principle, more electrical failures, often reported as electrical overstress (EOS) damages, than more robust components [11–13]. Here, the coverage and completeness of an ESD control program should also affect the MFR. Facilities not fulfilling all the control program targets should, in principle, have more electrical defects due to ESD.

The *White Paper I* proposes that an EPA having basic ESD control methods should be able to handle components with an ESD sensitivity of more than 500 V HBM [5,3]. Similarly, the *White Paper II* proposes that a basic ESD control program can protect

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components with more than 250 V CDM sensitivity [6,4]. More sensitive devices would need more detailed control programs with equipment ground connection, charging, and discharge control. Especially, when the CDM withstand voltage is less than 125 V a specific audit is needed to find root causes of ESD risks and to control those by process specific control measures [6].

In this study, the component HBM and CDM withstand voltage information is compared with electrical failure levels in an electronics assembly. In addition, ESD control program assessment results are compared with the electrical failure levels in those facilities in which the *ppm* values have been collected. Electrical failures can originate via several reasons; therefore, electrical failures due to ESD events are analyzed with risk estimation methods. The main purpose of these analysis is to evaluate how the HBM and CDM withstand voltage information reflects the real electrical failure levels and how the withstand voltage information can be used to optimize ESD control programs in an electronics assembly environment.

MFR data collection is presented in Section 2, results and risk assessment methods are presented in Section 3, the discussion is in Section 4 and a conclusion is given in Section 5.

2. Methods

2.1. Electrical failure reporting

To compare MFR values with the CDM and HBM withstand voltages, a high number of products and different components need to be analyzed. A component failure rate can be close to zero *ppm* when all the electronic manufacturing processes are stable, and it may require even millions of components to be assembled and tested in order to obtain statistically reliable data for failure analysis. In addition, a change in the failure rate may come from several sources, as there is always some normal process and component quality fluctuation affecting the MFR. This increases uncertainties with failure source analysis.

Electrical components are tested in the electronics assembly when the assembled and soldered printed circuit board (PCB) is ready for electrical tests. Especially, a reflow process can stress components due to a high thermal profile. This may initiate delamination damages and cracks on silicon or package layers, and the failure symptom of these can be reported as an electrical failure [14]. However, most of these failures can be classified as manufacturing process related with basic failure analysis. In addition, EOS failures can occur during PCB testing [12,14,15]. There can be several testing, programming, and qualification phases during final assembly and packaging phases. Here, the product or assembly is connected to test equipment via pogo pins or an interface connector is used to power and measure product functionality [16].

Test data need to be highly detailed to identify the real failed component on a PCB. The test data may have specific phases identifying different system functionalities run by IC components under investigation. One common test interface is the on-chip test access ports based on a joint test action group (JTAG) used to read registers and logic state of the ICs [16]. This can be used to filter electrical failures out of other failure signatures and give component-specific failure data. An in-circuit tester can be used to track failed components even without built-in test features or active circuits. A separate system rework phase gives component-specific failure data, as more detailed measurements and software tools can be used to specify the exact failing component. However, most electrically failed components are not going through detailed failure analysis. Full failure analysis are typically done by component suppliers only when a significant number of similar failures occur in electronics manufacturing or the component has a high-quality requirement. Failure analysis is also able to identify the type of failure but cannot always define a source of the failure in detail.

In this study, the IC is reported to have an electrical failure when a tester has measured a specific component parameter to be out of the accepted range and when a component replacement in a rework has restored system functionality. Other failure types are marked as process or handling-related and are not part of the statistics. Some of the reported electrical failures are also proved to originate from ESD events by component failure analysis and process risk assessments.

2.2. Source of data

The MFR data is based on 47 different products with a total manufacturing volume of about 150 million units between 2007 and 2015. The products were manufactured in 14 facilities having automated surface-mount assembly, manual and robot-based final assembly, testing, programming and final packaging operations. These facilities are located in Europe, Asia, and South and Central America. A total amount of different ICs handled during this period was about 6 billion. From these products, all ICs were used during a preselection phase to analyze MFR and ESD sensitivity data. Finally, 37 ICs were selected for detailed analysis based on the ESD sensitivity, availability of ESD sensitivity data, and reliability of the electrical failure reports. Most IC components with the 47 products had the ESD sensitivity equal to or more than 2 kV HBM and 500 V CDM.

Out of the 37 components, 13 were used in several products during the same period. In addition, one product could have one to six similar components on each PCB; thus, the total component count reported in this study is about 1.5 billion. Fifteen components out of 37 have the ESD sensitivity less than 500 V HBM and 500 V CDM. The most sensitive components have the HBM withstand voltage 100 V, and six components have CDM sensitivity equal or less than 250 V. These most sensitive components are RF devices directly connected to antennas with an operation frequency between 700 MHz and 6 GHz. However, the reported ESD sensitivity of an IC is set based on the most sensitive I/O pin [3,4]. Therefore, a component with, for example, a 1 kV HBM and 500 V CDM level may have only one or a few I/O pins with this level, and all the other pins or pin combinations are more robust.

The collected electrical failure data is an average of a daily, weekly, or monthly score. Daily or weekly data are used to evaluate sudden changes in the reported failure counts, and the monthly data are used to track generic trends with component quality. The monthly reports give statistically the most reliable results due to higher manufacturing volumes.

3. Results

3.1. Monthly electrical failure data versus ESD sensitivity

Component HBM and CDM withstand voltages are compared with average electrical failures in Fig. 1, where letters represent different IC components. The figure shows that most components have electrical failure values below 50 *ppm*, and only five out of 37 components have over 100 *ppm* values. The highest *ppm* values are with components *q* and *r* where the failure symptom is not ESD related, as the damages were related to software problems in a tester. In addition, the failure rate with components *s*, *t*, and *a* is not related to ESD damages but to other EOS events leading to thermal damages. These failures were caused by false power switching sequences and misaligned flex cable connectors. The long-term failure counts are the most important from the total failure cost point

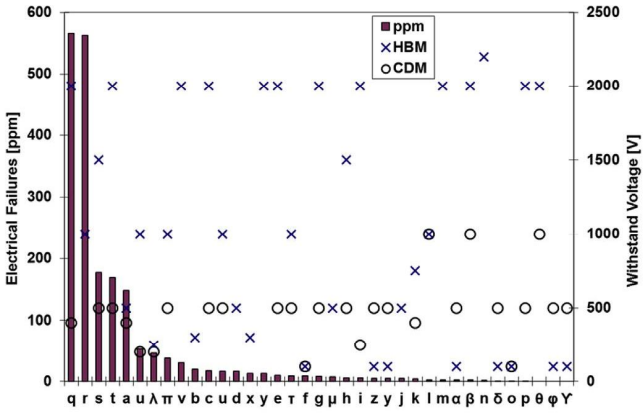

Fig. 1. Component HBM and CDM withstand voltages and reported electrical failures.

of view and will explain the generic trend with the component quality.

Based on the collected monthly level statistics from all ICs and the 37 ICs reported in this study, there is no correlation between the electrical failure data and component HBM or CDM withstand voltages. Both the ESD-sensitive and ESD robust components can have low or high *ppm* levels depending on the case. However, the challenge with long-term failure data is that EOS events leading to electrical failures may not occur with a steady rate or at a rate that makes the failure level visible. This is also the case with random or short period ESD failure events, which may not be visible in the monthly data. On the other hand, a modern electronics manufacturing is mostly automated and, due to systematic methods to handle sensitive components, ESD failures also can be highly repeatable; thus, changes with a *ppm* level can be easily noticeable even within a few hours or days period. The short time data can be compared with monthly levels, as shown in the example data set in Fig. 2. This figure shows that the monthly level *ppm* rates can be stable, and a typical fast increase up to 500–10,000 *ppm* can be easily observed when repetitive ESD events start to occur. However, the electrical *ppm* level can be higher when a new product comes to manufacturing. ESD can be one source of failures at this phase, but there are also typically assembly process related issues, testing challenges, and material quality related problems possible hiding EOS/ESD risks.

The same IC on a PCB can have varying electrical failure levels in different products. This is shown in Fig. 3, where the monthly *ppm* level and the HBM and CDM withstand levels are presented for 13 components identified by letters. Columns with a same letter show the *ppm* levels for each product. Here the data is not from the same period and the letters are not referring to the same components as shown in Fig. 1. In addition, manufacturing volumes vary between different products.

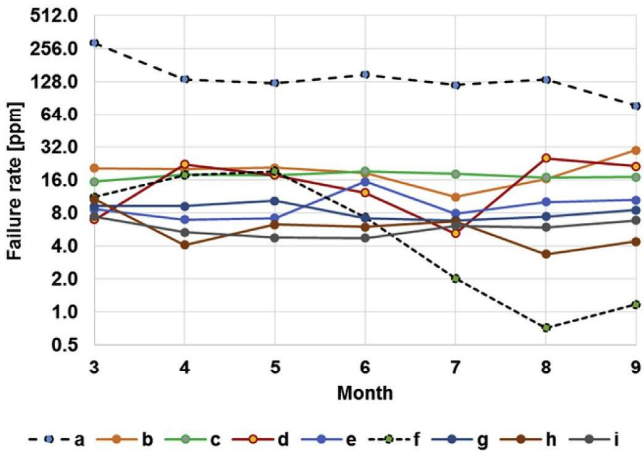

Fig. 2. Monthly MFR data for nine components.

The *ppm* level can vary between different products, even those that are produced on the same manufacturing line with the same tools and equipment. Here, the difference comes from varying PCB layouts, different mechanics used with the system, maturity of the assembly processes, and also from different testing methods and software used to operate the system. Once again, the electrical failures shown in Fig. 3 are mostly not related to ESD events but include other EOS failures originating from latch up, test software, and component electrical failures due to system or component package level design issues. With these 13 components, there is no correlation with electrical failures and ESD withstand voltages—even the total manufacturing volume of products was counted in tens of millions. It is, however, a good indicator of possible ESD problems when only one product or one manufacturing line will suddenly receive higher electrical failure levels with a specific component. For example, the component *j* has a significantly higher *ppm* level with two out of 15 products. Here the two products had CBE discharges in a programming station where the subassembly had static charges and on-board test pads were contacted with pogo pins. Later on, a field return rate of these two products dropped when the CBE in manufacturing was prevented, thus, a small part of the failures were not found by testing sequences used in manufacturing.

3.2. Weekly and daily electrical failures versus ESD sensitivity

Weekly or daily failure data show more details of the component failure counts but may not be useful if the production volume is too low to obtain statistically significant information. Anyway, a sudden increase in the electrical failure rate may be a signal of a possible ESD issue. In addition, the weekly or daily level quality data are able to prove the effect of corrective actions made on ESD control methods. This is shown in Fig. 4, where two separate ESD failure cases increased electrical failure levels from close to 0 *ppm* up to about 500 *ppm*. Arrows show the time when corrective actions were started. However, in these defect cases, several corrective actions were required, such as changing dielectric packages to dissipative and purchasing new ionizers, which took several weeks to implement and to be effective. When the source of ESD can be fixed immediately, the failure *ppm* level can drop faster, as shown in Fig. 5.

In Fig. 4a, the failing I/O pin in an IC had the ESD qualification level 1 kV and 500 V CDM, but the discharge current waveform was not similar to the ones measured during HBM or CDM qualification. The case in Fig. 4b was a system EMI disturbance due to an ESD event occurring in a few meters distance; thus, the level of ESD risk has no correlation with component-level HBM or CDM withstand voltages. In the case of Fig. 5, the problem was solved by changing test adapter material on a third day from dielectric to a dissipate type, thus preventing charge board event type discharges to occur during the initial phase of system programming. In this case, the failures were related to system-testing interrupts with no correlation with component-level ESD sensitivity.

The weekly or daily electrical failure data shows no correlation with the component HBM or CDM sensitivity data as the reported ESD defects cases occurred both with ESD-sensitive and ESD robust ICs. However, a majority of the found ESD events took place during the dry season with less than 45% relative humidity in EPA [10].

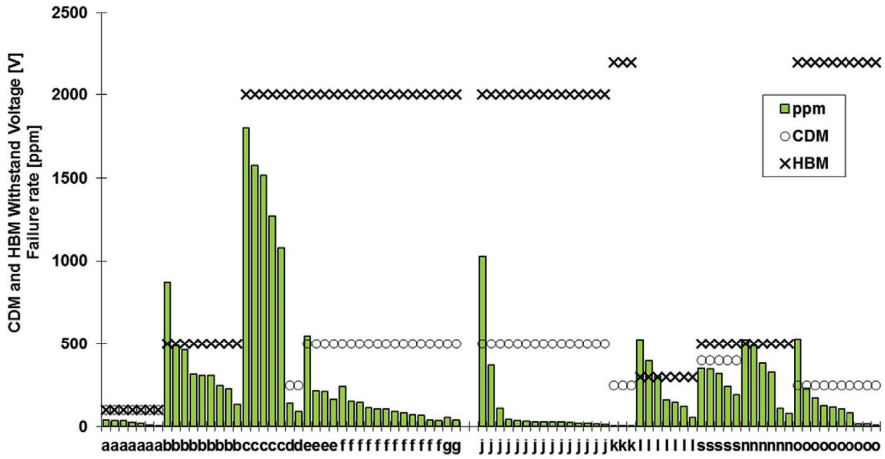

Fig. 3. Component HBM and CDM withstand voltages and reported electrical failures between different products.

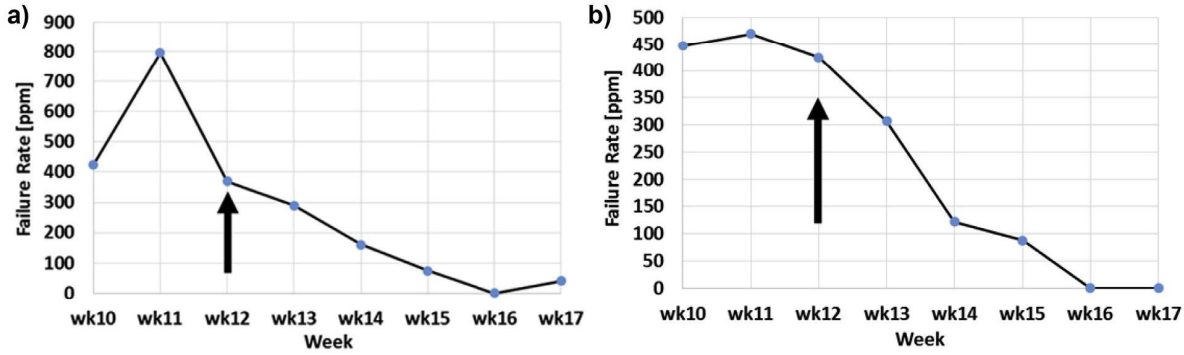

Fig. 4. a) Left. Weekly MFR data due to an ESD failure. b) Right. Weekly MFR data due to an electromagnetic disturbance.

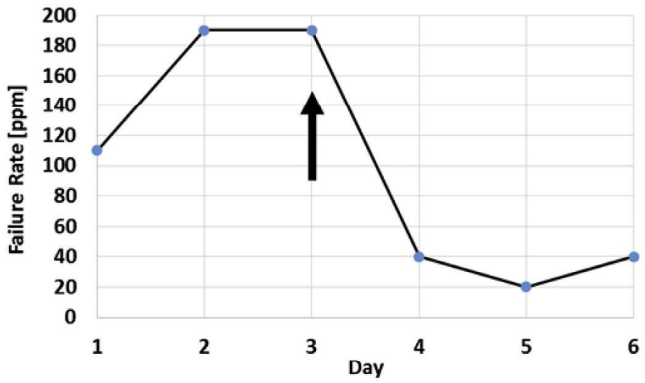

Fig. 5. Daily MFR data for an ESD case with a corrective action done on a third day.

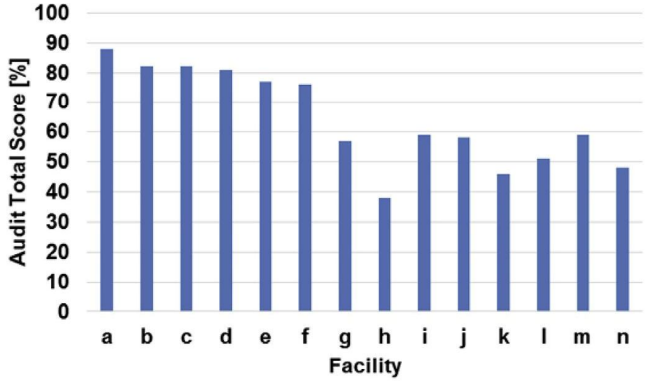

Fig. 6. Facility ESD control program audit results.

3.3. *ESD control programs versus electrical failures*

ESD audits were made for the same facilities between 2007 and 2015 from where the component electrical failure information was collected and the results are presented in Fig. 6. The control programs were audited against ANSI/ESD S20.20 and IEC61340-5-1 standard requirements with additional requirements for the control of product specific ESD risks. All the audited facilities had a minimum of a basic ESD control program established, which included, for example, floorings with below 10^9 Ω resistance, conductive shoes, equipment groundings, wrist straps for the operators, dissipative plastic trays with most ESDS, and an ESD control program documentation. However, there were major differences with the level of control documentation, ESD responsible competence, compliance verification methods, and additional product specific control methods. These facilities had different process equipment and different products under manufacturing, but most of the facilities had the same 37 components in use.

Facilities with a lower-ranked ESD control program had no higher electrical failure rates than those factories with a higher

program audit score with the same ICs. Instead, about half of the ESD-sensitive components had actually higher electrical failure levels in facilities *a* and *c* than in facilities with less than 60% audit score. This is mostly explained by Fig. 3 data, showing that the IC specific *ppm* level varies between different products.

During the data collection period, most of the audited facilities had a major ESD defect or system disturbance cases leading to major financial losses. These events occurred in high- and low-ranked facilities, but there were not enough failure events to use it for additional statistical analysis. Most ESD failures occurred with I/Os in multifunctional large processors and control ICs having multiple connections in a similar way as reported by Smedes [12]. More information of the events can be found from the Ref.[10]. It was also found challenging to link the level of an ESD control program to electrical failure rates or link the level of control programs to ESD failure cases in the audited facilities. One additional uncertainty is that the facilities had varying competences to detect and solve ESD risk.

3.4. Electrical failure probability estimation due to ESD events

In this section, ESD risks in electronics assembly operations are analyzed with *Design Failure Modes and Effects Analysis* (DFMEA) methods in order to understand how component ESD sensitivity could be related to the ESD events and electrical failure levels.

A typical electronic assembly contains several subsequent process phases. In addition, in one assembly line, certain slower process phases may have multiple parallel operations to balance phase output with the rest of the line. ESD failure cases in these phases can be analyzed with stochastic processes, which involve a sequence of random variables and the time series with the variables [17,18]. ESD events leading to damages in these phases can be dependent, partially dependent, or independent of each other. For example, a product assembly may get triboelectric charges in a process phase where the device is picked up from a tray. In the next process phase, the device is contacted with a conductive metal object, thus discharging the charge and possibly causing damage. Here, the process phases work independently, but both are required to realize the ESD event. Mitigating the ESD risk can be done in either process phase, but the best result would be obtained by preventing both the charging and discharging event.

The total failure probability of an assembly line or a system P_t can be expressed as $P_t = g(F_1, F_2, \ldots F_n)$, (1)

where function $g(\cdot)$ describes the relationship of each event F_i [19].

Each event in the process can be expressed by its parameters $F_i = f_i(x_1, x_2, \ldots x_n)$, (2)

where x_{in} define affective parameters for each function. These parameters x_{in} have a certain variation and uncertainty; thus, the event F_i is not constant. When all the affected parameters x_{in} are known, the F_i can be calculated. In addition, it also may be possible to estimate the events directly by using statistical data collected from the process. A product of the events will give the total failure probability P_t.

Fig. 7 shows typical functions and parameters estimating the probability of an ESD failure event based on equations (1) and (2) for an automated electronics assembly line. In addition, the realized risk level can be estimated with an additional function, including the failure severity or consequence of the failures. The functions can be explained with time domain probability expression information, as shown in the example data set in Table 1. The highest ESD defect probability is during the process step number 6, and there is only small change to produce other ESD events; thus, even some of the single functions would have a high event probability. In this example the step number 6 is a final assembly phase shown in Fig. 8 where a charged display is connected with a PCB. In parallel, several steps have zero defect probabilities due to the lack of static charges or because there is no metal-to-metal contacts with the assembly.

The component HBM and CDM withstand voltage directly affects only one of the parameters in Fig. 7. This is the sensitivity of the I/O in the *Design* function *F3*, but it is not always certain that the most sensitive I/O of the IC will be stressed during an ESD event [9,11,12,20]. In addition, there are a lot of uncertainties related to the HBM and CDM withstand voltages [8]. In reality, there can be more parameters affecting the probability of an ESD event; thus, the CDM and HBM withstand voltage define only one small part of

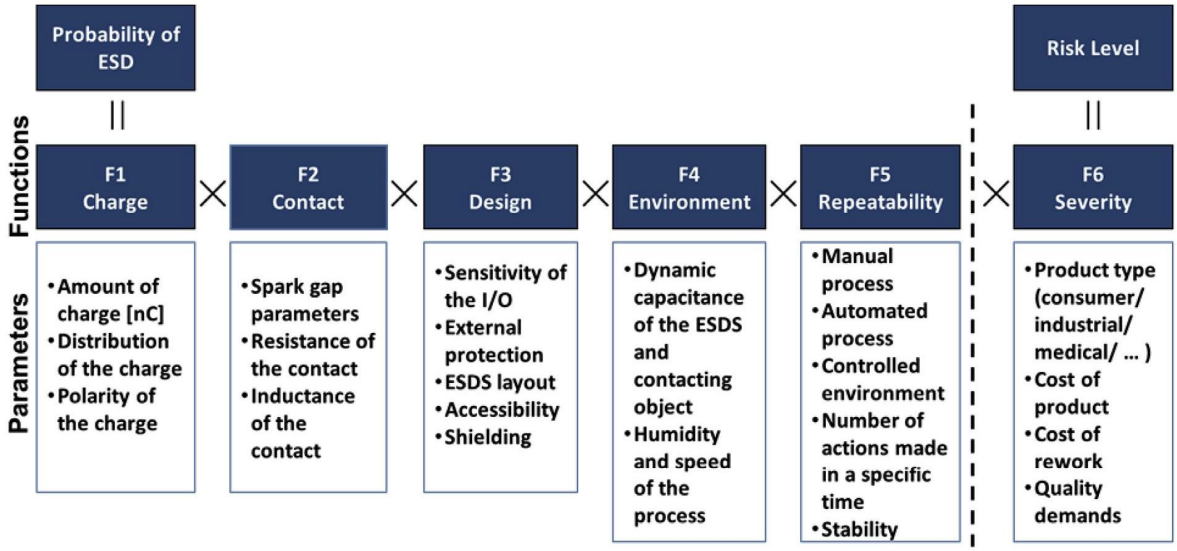

Fig. 7. Functions and parameters affecting on the ESD probability and realized risk level.

Table 1
An example calculation of ESD failure probability based on Fig. 7 functions.

	1	2	3	4	5	6	7	8	9	10
Charge	0%	0%	0%	5%	40%	20%	10%	5%	0%	0%
Contact	0%	0%	100%	100%	0%	100%	0%	0%	100%	0%
Design	0%	0%	50%	50%	100%	100%	100%	0%	0%	0%
Environment	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Repeatability	1005	100%	90%	90%	60%	70%	100%	80%	100%	50%
Defect Probability	0%	0%	0%	2%	0%	14%	0%	0%	0%	0%

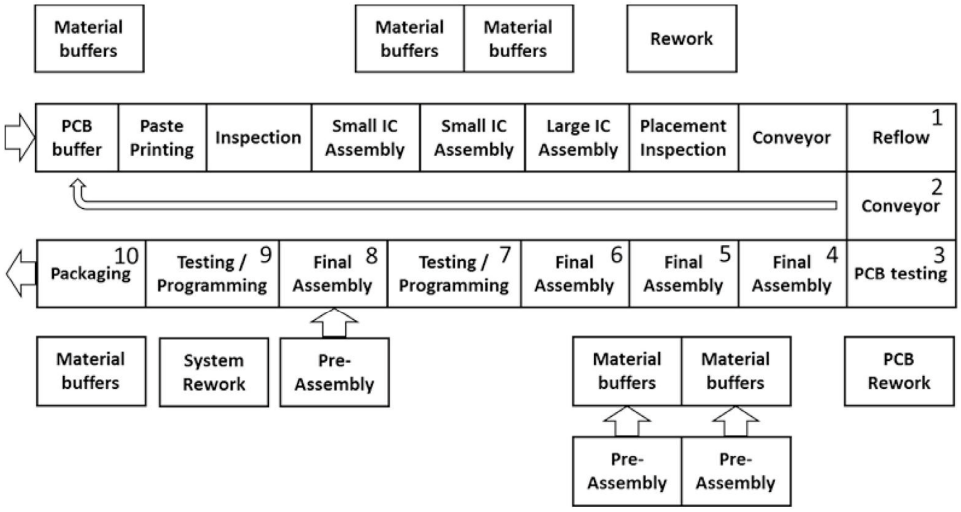

Fig. 8. An example layout of a single electronics assembly line with SMD, FA, and testing processes.

the total ESD risk scenario. A similar scenario could also explain the differences observed with component *ppm* levels between different products. Even with the same component the electrical failure rate may depend on other process or system-level parameters varying from product to product. Only when all the required prerequisites are realized in the correct order, the final result can be a destructive ESD event. Here, the HBM or CDM withstand voltage will play some role, but may not be the main criteria to prevent or trigger a failure scenario.

In this study, the most sensitive components have I/Os with 100 V HBM and 200 V CDM sensitivity. It is also possible that more ESD-sensitive devices with <50 V HBM or <100 V CDM would change the risk scenarios, and the I/O level sensitivity would become the most critical parameter. Still, this would only increase the probability of one function along the total ESD risk scenario, and mitigating the other affected functions would prevent the failure. This is more or less the current scenario with extremely ESD-sensitive magneto-resistive hard disk heads with less than a few volts withstand voltage [21]. These can still be manufactured without major EOS failures with proper control methods.

4. Discussion

Based on the analyzed data, electrical components with a low HBM and CDM withstand voltage do not have more electrical failures than more ESD robust components when the electronics assembly process has a basic EPA established. This was found when the ESD withstand voltage of the ICs is equal or higher than 100 V HBM and 200 V CDM. This supports the work and conclusions of the Industry Council on ESD Target Levels in *White Papers I* and *II*.

However, it is difficult to find a solid link between the HBM and CDM voltages and electrical failures. A component ESD sensitivity is reported based on the most sensitive I/O, and it is not likely that this I/O will be always along the discharge current path if ESD events occur in an electronics assembly. In addition, the discharge current waveform going through the IC may not be similar as used in the HBM or CDM qualification. There are also ESD-based failure and disturbance events in an EPA not directly linked to ESD sensitivity of electrical components but still affecting the yield of manufacturing and field return rates.

The reported IC specific electrical failure rate can be a low value below about 50 *ppm* due to stable manufacturing processes and high-quality components. However, there can be several parallel EOS events possibly increasing the electrical failure rate and ESD is only one of these. Therefore, ESD-based failures were difficult to separate from other EOS events from the collected MFR data. This is typically only possible when the source of the failure can be identified and failure analysis can prove a type of the damage. In addition, random failure cases due to ESD are difficult to find due to a low effect on IC's *ppm* levels. All these increase uncertainties when trying to link electrical failures to component ESD sensitivity.

To realize an ESD failure case in an electronics assembly always requires several related functions to be matched. These functions have varying parameters; thus, the probability of an ESD event will be a statistical phenomenon varying from case to case. The ESD risk event also can be a stochastic process where one sudden change with the manufacturing process will trigger a new ESD risk. This was supported by the observation that destructive ESD events occurred occasionally in all the 14 audited facilities under the study; even the ESD audit scores varied from 40% to 90%.

5. Conclusions

ESD risks and electrical failures in the electronics assembly

environment are not directly linked to the ESD sensitivity of ICs, and it can be misleading to define the ESD protection capability of an EPA based on the HBM and CDM withstand voltages of handled ICs. The situation may change if highly ESD-sensitive electrical components will be handled; thus, similar control methods as used in the hard disk industry may be required.

To further improve EPA performance, product and process specific risks need to be analyzed with additional control methods such as with the DFMEA. Here, the complete process flow needs to be analyzed by identifying risks and estimating or measuring the risk probabilities. This enables us to mitigate the risks before real failures will occur.

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Product Specific ESD Risk Analysis

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50 Words Abstract - Product and process specific ESD failures can be a challenge despite the well implemented EPA. An efficient ESD control program can be built when process specific risks are analysed based on product sensitivity. In this paper a method and case studies are introduced for controlling product specific ESD risks.

I. Introduction

An Electrostatic Protective Area (EPA) is a base stone for ESD control program and can prevent more or less ESD related failures originated from materials and humans. However, electronics manufacturers have found cases where even a well operating EPA cannot prevent ESD based product failures. In this case failures are typically occurring during product assembly and testing phase [1,5]. EPA precautions cannot either prevent Electromagnetic Interferences (EMI) to occur in the area. EMI can be originated from ESD discharges caused by charged product parts or from equipment used in the area [3].

Product robustness and process specific information is needed for ESD risk classifications. However, product or system level ESD sensitivity is typically poorly known during manufacturing. Component level HBM and CDM withstand voltage information cannot be used for system sensitivity classification and IEC61000-4-2 stress information may neither be available as this validation is typically done only for the final product [4]. IEC stress results can be also very different to the real world stress situations found in manufacturing and may lead both to overkill and underestimations of product specific ESD risks.

There are methods available which can be used to analyse process and product risks, product robustness and bring valid information for the control program. These methods base on process analysis, product charge and voltage measurements, electromagnetic interference (EMI) measurements, simulations, dynamic discharge event measurements and product sensitivity tests.

In this study we will present one procedure to define product specific risks by using process and product specific measurement data. The second chapter will explain step by step the procedure and the third chapter will present real world examples where the procedure has been used. Example cases show how control program and product design is tailored based on the risk analysis. Totally four example cases are presented in this paper. The first example is presented in details to explain the way of using the methodology. The next examples, which use the same baseline, are presented in general level.

II. Risk Analysis

Target of ESD robustness analysis is to get information about product ESD sensitivity for handling, manufacturing and R&D purposes. The sensitivity can be a maximum stress level products can withstand in the worst case environment. The sensitivity can be validated also in a fixed discharge environment, similar way as with component level HBM and CDM validation. Another option is to specify the sensitivity as a maximum stress level the product can withstand in a real discharge event found in handling and processing environment. This real case option is more efficient as typically products are not stressed in EPA with the worst level stress. The worst case scenario would most likely lead to overkill with ESD control program. Taking the varying discharge environment into account can be a major benefit with product level risk analysis. A drawback of this principle is the fact that product specific ESD risks and sensitivity is valid only in the specified process and needs to be analyse separately each time the process or product will change.

A. Procedure

Process and product risks are analyzed step by step as follows:

a) The first step is to analyse manufacturing or other target processes and to find possible ESD risks. A good way is to follow the process critical path where ESD sensitive assemblies are handled [5,6]. This can be done by searching ESD events from the process for example with EMI event detectors or with antennas and oscilloscope. However, there is typically also non-ESD related EMI noise in manufacturing and additional analyses are needed to locate and classify risks. Maximum potential V and charge Q can be measured from product parts with

metal structures and from other possible electrostatic source circuits. Based on the given information quasi static parameters such as capacitance and potential energy can be calculated. Electrostatic fields can be measured when dielectric materials are used in the process or the product itself has dielectric surfaces.

It is important to note that ESD risk level is typically very low when a charged ESDS discharges to a person via finger contact. Finger contact has relatively high resistance and ESDS parts have typically low source capacitances. These two parameters limit typical ESD stress energies. In addition, as the contact is made in EPA, we can assume that the operator potential is close to zero during handling.

b) The second step is to analyse discharge contact parameters (metal-to-metal contacts) and dynamic capacitance of a charged object during a discharge event. For example, a plastic cover with non-grounded electromechanical parts can touch on a sensitive contact pin on PCB during assembly. This contact may have totally different RF characteristics than in a case where a charged PCB is discharged through a grounded support pin. A non-grounded small metal part can typically discharge only part of the charges and ESD stress will be weaker.

It is also important to define the dynamic RF capacitance (C_{ESD}) of the discharge event. The discharge is totally different if a charged and isolated ESDS is discharged when it is placed on a thick dissipative material or when it is on a metal surface with thin dissipative coating. In the latter case RF capacitance is much higher than DC capacitance causing magnified ESD stress as shown in Figure 1. Unfortunately, the dynamic capacitance cannot be determined with static potential and charge meters. RF capacitance can be estimated by integrating discharge current, charge and energy with an oscilloscope [2].

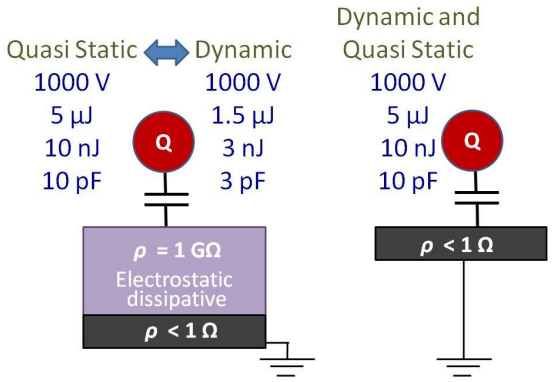

Figure 66: Dynamic and quasi static discharge event.

c) The information collected in the previous two steps is now used to construct a similar discharge environment for a product sensitivity test. Here a test bench is needed and it can be built up by using metal plates and dielectric or dissipate sheets [4]. It may be also possible to use real product specific adapters or jigs in a test bench, but very often those items cannot be removed from the process. An example of a test bench is shown in Figure 2. In this bench, PCB is placed on a high voltage metal plate isolated by 0.1 mm thin dielectric film, causing a high capacitance environment for a charged board event. PCB is charged up by influence of electrostatic field. This simulates an environment where a PCB is contacted with a tester pogo pin having 100 nH inductance to the ground.

Figure 2: Test bench to analyse PCB robustness.

d) The next phase is to stress ESDS with different potentials and charge levels on the selected contact points. The discharge must be made in a similar way as it happens in a real world process. The best accuracy can be reached when discharges are made with the real contact item such as a wire, a mechanical part or another ESDS. The discharge can also be made with a ground wire having chosen RF parameters. In this case the discharge waveform can be measured with a current probe, as shown in Figure 2. Current measurement provides also additional information such as peak current, rise time, waveform frequency and inductance.

e) Product part robustness is specified by using discharge waveform information or by using parameters which the test bench provides. For example FICBE (Field Induced Charge Board Event) method provides capacitance, potential, charge and energy information without current waveform measurement [2]. It is essential to specify the part robustness with all known parameters – not only with potential. It is also important to note that electrostatic fields, potentials and charges are the only parameters which are typically measured in a real manufacturing process with basic hand held tools. Product part

withstand parameters can be given for example as shown in Figure 3.

f) When the sensitivity of the product part is known it is time to go back to the manufacturing process and verify that product potential and charge levels are less than the measured values. For example, a product failed in a test bench with 1500 V & 20 nC, but when it was measured in manufacturing only maximum 750 V & 10 nC was found. Even if EMI detector would indicate repetitive discharges during production any changes to ESD control procedures may not be needed. However, it is important to realize statistical aspects and possibly changing environmental conditions.

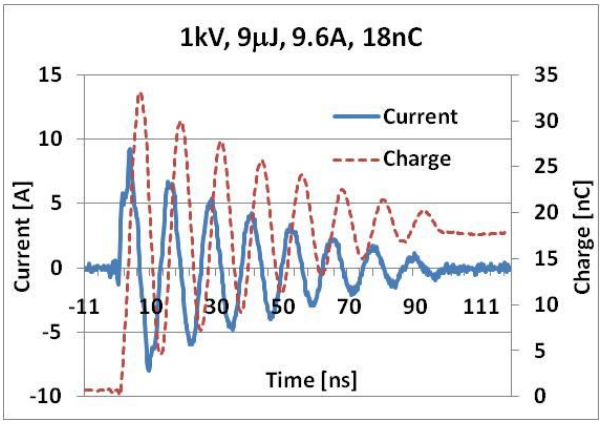

Figure 3: Product sensitivity information.

III. Example Cases

A1. Antenna Discharge

A component radio Tx I/O was found to have decreased attenuation in a tester after product mechanics assembly phase. The damaged I/O was directly connected to the product antenna mechanics and there was no on-board ESD protection on PWB layout between the I/O and the antenna contact pad. The component Tx I/O had relatively high on-chip protection level; 2 kV HBM and 750 V CDM. Component failure analysis revealed oxide breakdown failure structures in a capacitor area as shown in Figure 4. This was most likely occurring due to excess voltage stress and ESD was a main suspect. ESD risk analysis were started to resolve the case.

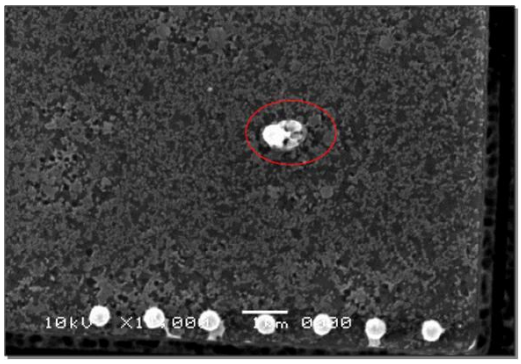

Figure 4: An oxide breakdown failure

The only phase where the I/O had a change to get ESD stress in manufacturing was the assembly of cover mechanics. Cover was made of plastic and had several integrated electromechanical parts and antenna structures. PCB and cover were placed together manually in a grounded adapter having 4 mm thick dissipative bed on a metal frame according to Figure 5. The adapter had not any metal-to-metal contacts with the product parts. Other basic EPA protection methods were also taken into account, such as grounding of operators and workbench surfaces.

Cover part was not classified as ESDS and was transported on a dielectric tray to the assembly area. Both the tray and cover had high surface charge density due to triboelectric charging. Potential of the cover part was typically between 0 V and -500 V on the adapter. Dissipate tray was also tested, but it was found that the dielectric cover charged about to the same level during handling both with dissipative and dielectric trays. Therefore, the tray had finally no effect on the final charge levels.

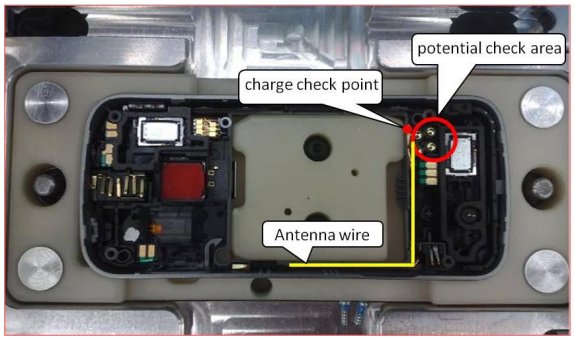

Figure 5: Antenna mechanics in a cover part

ESD risk analysis was started by detecting random EMI events when a cover was placed on a PCB. Potential of the cover and antenna was measured with a non-contact voltmeter. Mobile charge was measured directly from the antenna metal wire with a Monroe nanocoulomb meter, Figure 6. It is important to note that the charge and potential values

seem not to correlate so well. This is mainly due to inaccurate surface potential measurement with plastic parts. Here the potential meter was measuring the average *E*-field above the part and the measured area was also wider than the antenna itself. Therefore, we decided to use charge value alone for risk classification as the charge measurement has better accuracy when meter leakage is minimized.

The next step was to measure the dynamic parameters of the antenna wire when the cover was in the adapter. Antenna was charged to a known potential and discharged to the ground through the Tektronix CT1 current probe. Charge was integrated from the current waveform. Dynamic capacitance of the antenna wire was found to be about 1.4 pF. Quasi static capacitance was about 4 pF. PWB capacitance was > 20 pF and was thereby able to discharge the antenna wire charges completely through the Tx I/O when connected together.

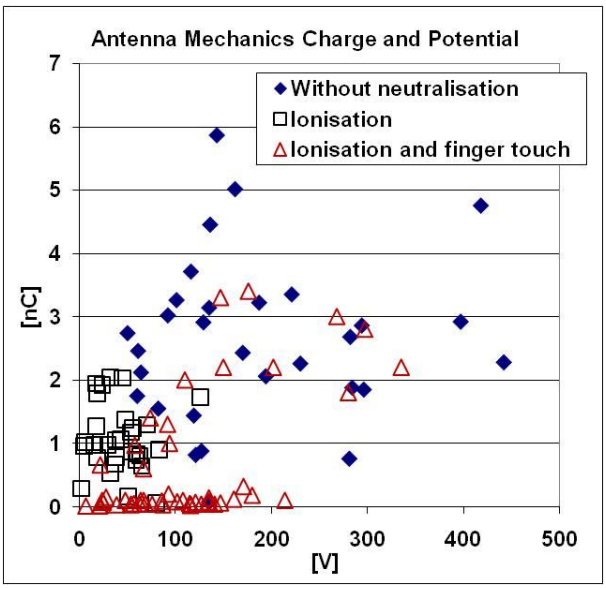

Figure 6: Mobile charge and potential of the antenna mechanics.

The next phase was to analyse the discharge waveform with different stress levels when a charged antenna wire was connected with PCB. The cover was placed on a test bench shown in Figure 2 and the dynamic capacitance of the antenna was adjusted to 1.5 pF by changing the dielectric thickness between the cover and induction plate. Induction plate voltage was altered in such a way that the antenna charge in nanocoulomb was in the same range as seen in Figure 6. CT1 current probe was used to capture the waveforms on different stress levels. Induction voltage was changed in 500 V steps and two example waveforms are presented in Figure 7.

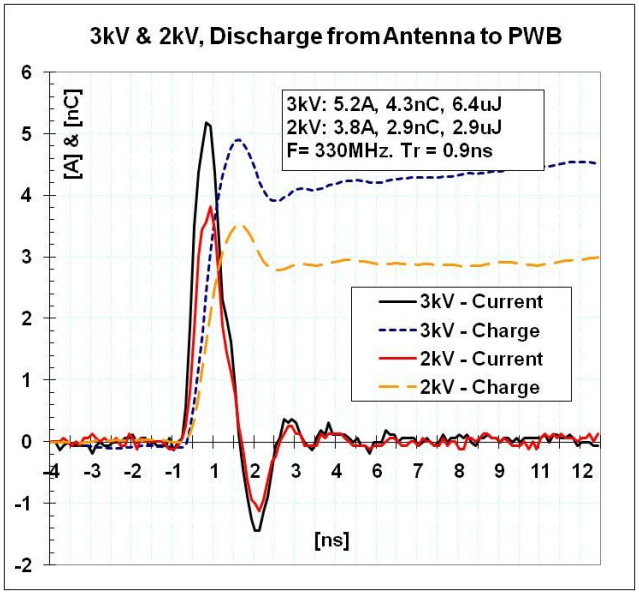

Figure 7: Antenna discharge.

Tx I/O got the same attenuation as found in the real process when the peak current was more than 5 A, the induction plate potential was more than 3 kV, the mobile charge was more than 4 nC and the transferred energy was more than 6 µJ. Multiple discharges were able to produce the same failure due to cumulative stress when the current was more than 4 A, the charge was more than 3 nC and the energy was more than 3 µJ. Tx I/O was stressed also with IEC61000-4-2 method and failures were found with about 1…2 kV stress pulses. IEC test results had higher uncertainties due to the stress voltage and discharge contact variation.

A2. Antenna Discharge - Summary

A product specific ESD risk analysing method was used to solve the component failures. ESD was found to be the main reason for Tx I/O failures and the failure was generated by the antenna mechanics assembly. The antenna wire had typically charges between 1 nC and 6 nC while neutralisation was not in use. This was more than the maximum safe values of Tx I/O according to the stress test results. Ionisation and finger touch neutralisation were tested, but efficiency of charge removal depended on the operator and over 3 nC charges occasionally remained in the antenna. Random failures were found even both the ionisation and finger grounding methods were in use.

A surface mount resistor was added to PCB layout to protect Tx I/O during antenna assembly. This solution alone solved the case and any changes to ESD control process were not needed.

B1. Flex Component

The second example case is a flex PCB subassembly which had a high electrostatic charge during assembly phase. This subassembly part has several ESD sensitive components on the board; light emitting diodes (LED) and HALL magnetic field sensor components on the top surface. There is also one optical sensor IC component having 8 kV ESD withstand voltage based on IEC 61000-4-2 waveform.

The flex part charged up in a vacuum assisted assembly adapter when a dielectric protective foil was peeled off from the component surface. The assembly adapter was made of dissipate material and the flex component had dielectric material on all surfaces. The potential of the flex was measured to be between 30 V and 600 V when it was in the adapter. Maximum electrostatic charges in flex traces measured with a nanocoulomb meter were over 40 nC. This was an indication of high charging and relatively high capacitance between the flex and ground, approximately 70 pF. Calculated potential energies were over 10 µJ. Capacitance of the flex increased close to 1 nF when a vacuum was turned on and the flex moved close to the adapter surface. All these parameters represent a quasi-static situation.

There was a discharge between the charged flex component and the product main PCB when those were assembled together. Since the quasi static parameters may not explain real world ESD risks, dynamic ESD measurements were made with ESD event receiver [2]. During ESD event, the capacitance of the source circuit (flex component) was found to be only 10 pF, the maximum transferred charge 2.5 nC and the discharge waveform frequency about 10 MHz, Figures 8 and 9. The measurement results were verified by using 100 Ω and 1500 Ω resistance in a discharge network. 100 Ω simulates a discharge event with the main board contact and 1500 Ω a human touch discharge. We can see from Figure 10 that the discharge via a human hand kind of contact has only about 30% of the peak current level and five times longer main discharge period than the main board discharge seen in Figure 9. Therefore, a discharge between the main PWB and the flex component is the main risk event from ESD protection point of view.

B2. Flex Component - Summary

Despite the relatively high quasi static potential energy, the dynamic ESD energy remained in a low level according to Figures 9 and 10. Any changes to ESD protection was not made as the measured dynamic stress was less than ESD sensitivity of the flex component.

Figure 8: ESD parameters capture with ESD event receiver.

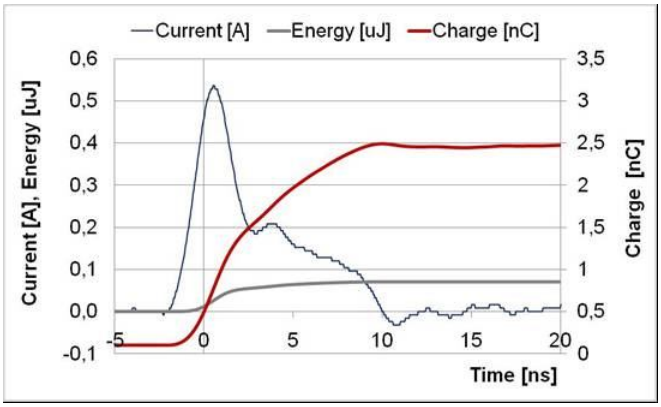

Figure 9: ESD parameters captured from flex with *100 Ω* CDM discharge network in a receiver.

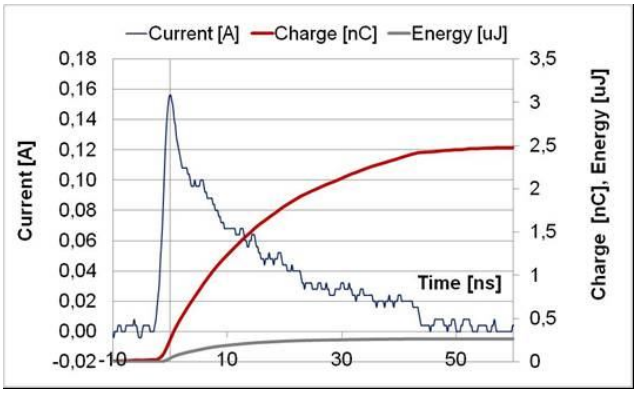

Figure 10: ESD parameters captured from flex with *1500 Ω* HBM discharge network in a receiver.

C1. Window Component

The third example is a case study made for product design purposes. A window subassembly component with integrated touch sensor drive IC charged to a high potential when a window protection foil was peeled off from the surface. This tape was used for

contamination control during manufacturing and was removed just before assembly, Figure 11. Component surfaces had dielectric coatings and high surface potentials were found both top and bottom side. The component was designed to withstand more than 15 kV IEC 61000-4-2 stress when it was connected to a product and would have all the ground connections in place. However, it was still unsure if the component would be ESD sensitive when it was assembled to the main product via a connector and ESD would happen between the parts. In this situation the product would not be protected by the ground connections and the discharge current would flow through different paths.

Figure 11: Window component with a touch sensor.

The window component was placed on an assembly jig and the protection tape peeling was repeated tens of times. The component charged up to maximum 600 V and the maximum quasi static charge was about 20 nC. Dynamic discharge parameters were analysed with an oscilloscope and Tektronix CT1 current probe. As a result, 30 pF dynamic capacitance and a ground wire with 80 nH inductance was found to produce the same waveform as would happen in a discharge between the main product and the window.

The selected discharge parameters were set to the test setup shown in Figure 2. The test bench was used to induce different stress voltages into the component. Component was also tribocharged by peeling off the tape and discharge waveforms created both with the induction and tribocharging methods are compared in Figure 12. Component charging varies a lot when tribocharging is used, but as shown in Figure 12, the discharge waveform is about the same when discharge environment is fixed. Induction charging is more accurate to repeat and a discharge with 500 V induction level had the following discharge parameters; peak current 6 A, transferred charge 15 nC and discharge energy 4 µJ.

The next step was to analyse the window component ESD sensitivity with similar stress waveforms. The component was stressed up to the failure point and operation parameters shifted when the discharge had peak current more than 15A, transferred charge 45 nC and discharge energy approx. 30 µJ.

C2. Window Component - Summary

The component had clearly lower ESD stress levels in a real world assembly process than the measured failure level in a test bench. Based on the measurements, any extra protection or product design changes were not needed for the assembly phase.

It is also important to note that there was not any correlation between 15 kV IEC validation results and the failure level found in the test bench. This was most likely due to different dynamic stress environment, ESD waveforms and stress contact points between the test methods.

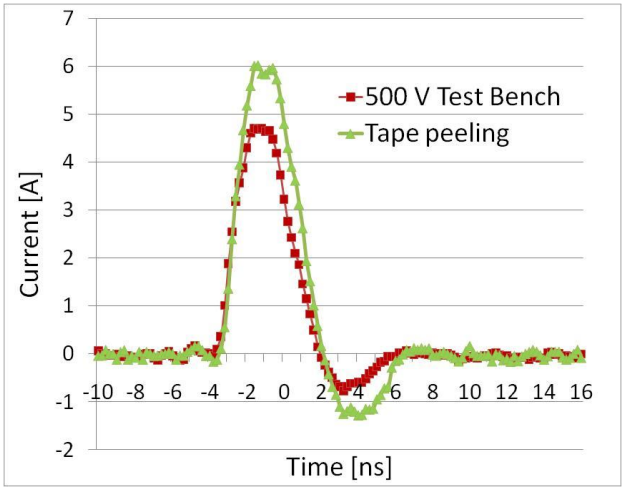

Figure 12: Discharges from the window component.

D1. EMI disturbance

The fourth example is a case study where EMI pulses were found in manufacturing area with oscilloscope and loop antenna measurements. There was a random EMI pulse detected when products were placed manually on to programming station adapters.

Products had dielectric plastic covers and those got triboelectric charges during handling. The charged covers induced an electrostatic potential on conductive parts of the electronics and this charge was discharged into the ground when products were placed into the adapter, Figure 13. The product was not damaged in this ESD event, nor was disturbed from the EMI, but programmers close to the discharge point were not able to tolerate EMI pulses. EMI coupled into a non-shielded clock signal cable and an example distortion shown in Figure 14 was measured with the oscilloscope. The raising edge of the clock pulse was lost and data transmission was stopped.

Products were measured with a non-contact voltage meter when those were placed on to the adapter, Figure 13. A typical potential curve showing the approaching product and the ESD discharge event when the product is contacted with a adapter pin is presented in Figure 15. The measured potential and the strength of detected EMI pulses varied a lot depending on the tribocharging effect with the covers. Products had maximum 40nC charge when the discharge event happened and the potential in the metal areas varied depending on the product capacitance.

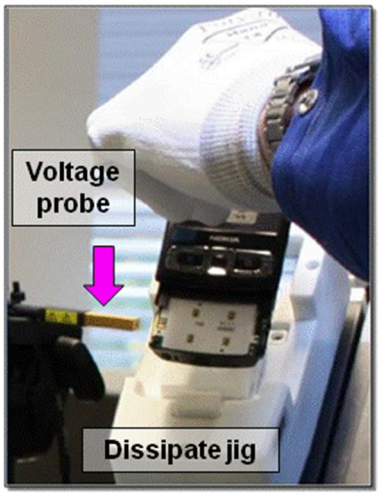

Figure 13: Product potential measurement

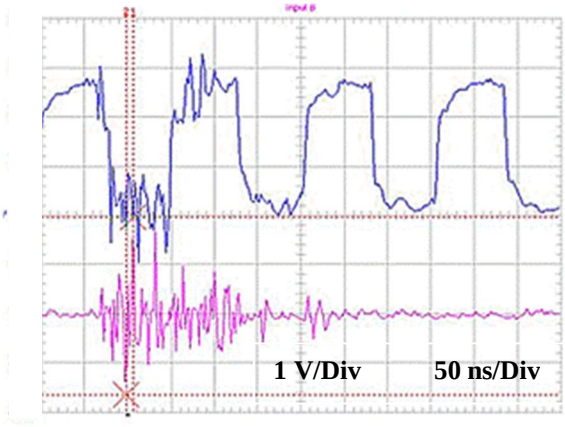

Figure 14: EMI pulse and a distorted clock signal.

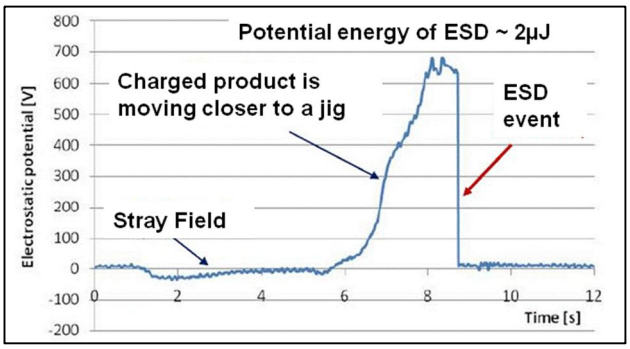

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Figure 15: Product potential during the assembly operation.

D2. EMI disturbance - Summary

The discharge happened between the product ground layer and the ground pin of the adapter. This was a safe discharge event from product point of view. It was also challenging to neutralise the product and to solve the case it was decided to try to improve programming station EMC immunity. Signal cable was changed to a shielded type and this alone was able to prevent EMI coupling into the clock lines.

IV. Conclusion

ESD risks are typically controlled by implementing an EPA in manufacturing. Unfortunately, EPA alone cannot prevent all ESD failures as handling and processing charges dielectric product parts. Product specific ESD risks can be controlled with systematic process risk analysis which bases on product robustness information and process measurements. These analyses should be done to all new products and processes where ESD sensitive electronics will be manufactured.

Four examples of such a risk analysis were presented in this paper. In the first example high charges in antenna module caused changes in RF component operation. This was solved with product design changes. The second example had a flex PWB component with high charges. In this case the dynamic discharge parameters were found to be less than the level required to cause ESD failures and no changes were required in the assembly process or with product design. The third example had a case where product design was supported with ESD sensitivity analysis. In this case the component was found to be ESD robust and any changes to the product design or assembly process were not required based on ESD stress tests. The last example case was EMI disturbance where products were not having any damages, but programming stations nearby had disturbances. This was solved with improved programming station signal cable shielding.

All the presented example cases are not covered by basic EPA control methods and cannot be prevented by the generic ESD protection programs. By measuring product and process specific ESD risks with systematic methods we can detect and prevent ESD events and also support product R&D with ESD protection design. This requires typically potential, charge, discharge and EMI control in the controlled area.

Discussion

In principle, it could be possible to control ESD protection alone with a detailed product and system level risk control. However, without EPA changes in the process environment or human way of operation would create new unpredictable risks. Therefore, EPA is still needed and product and process specific analyses should be understood more as an extension for an existing ESD control program build according to IEC 61340-5-1 or ANSI/ESD S20.20 standards.

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ESD and Disturbance Cases in Electrostatic Protected Areas

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ESD and Disturbance Cases in Electrostatic Protected Areas

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50 Words Abstract – Electrostatic protected area (EPA) can effectively prevent ESD failures from charged operators, work benches and tools. However, electrical disturbances and ESD events from other sources can still exist in well-built EPAs. In this paper failures found in electronic assembly environments are analyzed to improve coverage of ESD control programs.

I. Introduction

ESD Control Programs based on ANSI/ESD S20.20 and IEC 61340-5-1 standards have the main focus on administrative and technical requirements of ESD control program and can provide an efficient environment to minimize ESD risks [1]. The coverage of these programs can vary from mostly image and show, to a more technical oriented approach [2,3]. Both of these program types can be fully compliant with the ANSI/ESD S20.20 and IEC 61340-5-1 standards as there are many ways to implement a program.

ESD Control Programs should be built based on the required protection level. The level of optimal protection depends largely on the type of electrostatic discharge sensitive components (ESDS) and the way ESDS are handled. In a manual handling process a basic control program can prevent more or less all ESD event based failures. However, when the handling processes contain widely different electrical products, mechanical components with dielectrics, and automated processes, some of the possible discharge risk scenarios may not be fully covered. One of the challenges is to detect and define the optimal level of ESD control required in each case.

When all the basic electrostatic protected area (EPA) precautions such as grounding and dissipative packaging materials have been established, additional ESD protective actions and process optimization tasks can still be done to improve the process yield and efficiency [2,4,8]. This requires some knowledge of the possible ESD related risk scenarios.

In this paper we present some major ESD and Electromagnetic Interference (EMI) failure cases found in EPAs. Here a failure means that significant amount of products have suffered electrical damage or the process yield has decreased due to testing or programming defects. These cases have been found by the authors in electronics assembly environments in different companies over the last 10 years. All these cases have occurred in EPAs mostly meeting both ANSI and IEC standard requirements, and the analysis bases on 42 individual failure cases fulfilling the criteria to be used in this study.

The presented distribution of failure cases and failure sources represents mainly electronics assembly processes in industrial, commercial and medical electronics area. The companies have been mostly medium or large size. Different failure distribution data may be found for example in a small scale manufacturing, semiconductor, automotive or aviation electronics manufacturing processes, where the type of ESDS, construction and handling of ESDS can vary. In this study component assembly phases have been fully automatized and most of the mechanical assembly operations were done manually, but also fully automated processes are included. The cases are collected from manufacturing sites located in Europe, Asia and South America.

The main purpose of this paper is to analyze the type and reason of the observed failures and thereby produce information to further improve ESD control programs and electromagnetic compatibility (EMC) related risk prevention in an electronics assembly environment. We will first present statistical data of the major ESD and EMI related failure cases in Chapter II. The data is further analyzed in Chapter III. We will discuss and show example methods found useful to minimize the observed failure cases in Chapter IV, and results are summarized in Chapter V.

II. Failure case analysis

A. Source of failures

The failure cases are analyzed by using three categories; source, event type and victim. The first category explains possible sources for failures based on the following items: static E-fields, ESD, EMI, External Power Supply (EPS), and a High Voltage (HV) source. The observed failure sources with the

percentage information of the total are presented in Figure 1.

EPS is understood in this study as an external electrical power source such as a battery or a charger. The source is categorized as EPS when the event has included for example excess DC/AC voltage or wrong polarity plugging of the power source. These events can be initiated by an ESD event or EMI pulses, and in this special case the failure event include both sources.

The largest failure group in Figure 1 is ESD, which has been categorized when a direct ESD between the victim device and another object has caused the failure event. E-field is the source for example when an electrostatic force cause failures. HV is selected when the voltage alone is the source of a failure. HV and EMI are categorized as the source when, for example, HV cable sparking generates EMI pulses and the radiated RF noise disturb equipment operation.

The list of possible sources considered here has not included charged humans, seats, tables or other similar basic controlled EPA items. These were already well under control in the EPAs where the data was collected. The authors experience is also that failure cases from these sources are extremely rare and random in well controlled EPAs. It is also challenging to separate these from other possible electrical failure sources due to the low rate of occurrence. On the other hand, this experience supports the view that EPAs built based on current standards can effectively prevent these kind of failures.

B. Type of failure events

The second category shows a statistical distribution of failure event types based on the commonly used models; Human Body Model (HBM), Charged Device Model (CDM), Machine Model (MM), Cable Discharge Event (CDE), Latch Up (LU), and Charged Board Event (CBE). These events involve an electrical contact with charge transfer occurring. In addition, we use two additional event types based on Electrostatic Attraction (ESA) and failures due to radiated RF noise marked with EMI. The type and share of failure events is presented in Figure 68.

HBM is a discharge event between a human hand and ESDS, and MM represents a discharge from a charged conductive large equipment or mechanism. CBE and CDE include discharges from a charged ESDS assembly and also discharges between charged mechanics/cables and the ESDS. CDM is an event occurring when a single integrated circuit (IC) component touches conductive material with a charge transfer. ESA events are related to material sticking on charged surfaces and malfunctions caused by electrostatic forces. In a LU case the failure event is related to the excess current and voltage from a power source. The last event type EMI is a narrow or wide spectrum signal coupling into equipment or the product itself. Here only transient high amplitude signals with high power density are counted, thus, continuous low amplitude RF noise is excluded.

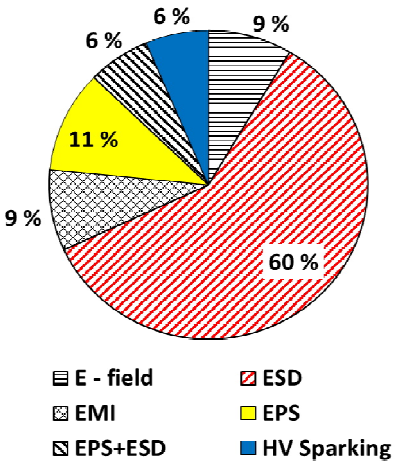

Figure 67: Observed failure sources.

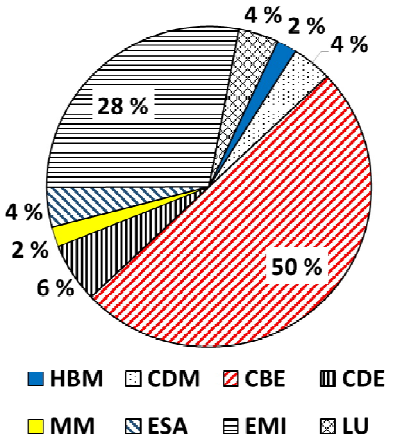

Figure 68: Event type leading to a failure.

C. Failing parts

The third category is the type of failing victim in EPA based on the first and second category. However, it is not always as straightforward to define a single victim for a failure. For example, RF noise can couple via a cable and through several components on a printed circuit board (PCB) before it reaches the IC that may finally produce the failure. Therefore, a specific IC has been selected to be the main victim only when failure analysis have proven the failure to exist inside the IC. In other cases the victim is

selected based on the module where the failure was observed. A sensor and display module are selected as their own group as those can be typically tested separately, and a whole system is marked as the failing part when more detailed information is not available. In addition, electrical testers and equipment used in the process area are counted as one group.

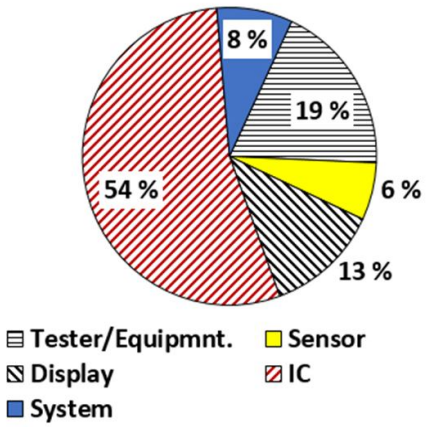

Figure 69: Failing items.

III. Failure case analysis

Figure 67 shows that more than half of the observed failure sources in EPA have been ESD events even though the EPA might be expected to prevent ESD from taking place. EMI and problems with power sources represent together about 25 % of the observed failure sources. Static E-fields and HV sources represent less than 15 % of the cases. This analysis suggests that a typical ESD control program may only partially cover E-field and ESD event detection, whereas HV sources and EMI detection can be easily overlooked. EPS sources can be challenging to detect as these depend strongly on the type of products and equipment used. In our experience the external power source has typically been a product tester, battery or programming equipment. Here the correct operation of software plays also a major role as the failure may occur only when the product is in a specific operation mode.

CBE is the most common failure event type in Figure 68. This is not surprising as subassemblies, PCBs and mechanical components are the most common parts handled in electronics assembly process. EMI events represent about one third of all the events leading to failures. This is consistent with the several testing phases typically required during electronics assembly, programming and qualification. Some of these testers are often built in-house and are not subject to EMC immunity or emission qualifications. The process area may also have a high variety of tools and equipment producing periodic EMI pulses or radiating RF noise to the close environment. Therefore, ESD or LU events are not the only source or event type leading to EMC related failures in an EPA.

The rest of the events in Figure 68 represents each less than 6 % of the total. However, HBM, CDM, MM, LU, CDE, and ESA together cover about 20 % of all the failure events. Therefore, it is important to evaluate these event types when optimizing EPA control.

An extremely high number of automated IC assembly operations has produced only very few CDM related failures. The data source used in this study includes billions of assembled components with less than 200 V CDM rating. The low number of CDM failures shows the low risk of ESD damage in the surface mount assembly processes used in most electronics assembly operations. In these processes ICs are kept inside tape and reel packages until the IC is picked up by a nozzle for assembly. CDM risk seems to be successfully kept low in the assembly phase by control of package materials, resistive solder paste on PCB pads, and capacitive coupling between the IC and PCB prior to a component placement [7].

There is also one HBM event in Figure 2. In this case the source of the event was a charged system periodically discharging into a neutral person with mega Ohm range grounding. Thus, the discharge event was similar to a real life HBM, but the source of the failure was not a charged person.

Figure 69 shows that in about 50 % of the failure cases one specific IC in the product was found to be the main victim. The failure was due to a physical defect or a major electrical disturbance leading to a product failure. In addition, electrical testers and equipment have failed in about 20 % of the cases. This is once again related to the amount of EMI events and number of testing phases occurring in the EPAs.

Displays and other electrical sensors have failed in about 20 % of the cases. Many of the electrical systems have a display or sensors integrated, and these can be susceptible to both ESD and electrical disturbances due to EMI. In electronic assembly these components are still open and accessible for processing which increase ESD and EMI risks. Displays contain also large dielectric plastic or glass surfaces that can be easily charged for example by peeling off a temporary protection film. These surface charges may trigger ESD or ESA events leading to product failures.

The rest of the failures in Figure 3 are counted as system level. In this case the failure has been a

complex combination of mechanics and electronics and it has been challenging to define a single failing component.

IV. Optimization of ESD control programs

According to the observed failure cases the greatest benefit for current ESD control programs in electronics assembly environment would come from enhanced CBE event control. In addition, expanding the basic ESD control on EMI pulse detection and mitigation would prevent major part of EMC related failures. This would not yet require expensive tools or specific competence, which is typically needed when RF signals or low amplitude RF noise is measured. Here a basic hand held EMI detector gives valuable information, and an oscilloscope with a dipole or loop antenna is able to measure the amplitude and position of the EMI pulses [5,6].

The challenge with CBE control is with the high variation of different assemblies and processes to cover. ESD sensitivity of assemblies is typically unknown and some of the assemblies may come from subcontractors without ESD sensitivity information. Products can also have varying process steps including product specific test phases. Here one way to optimize the control is to use a critical path principle, where detailed risk analysis is done only in those phases where assemblies are handled [2,3,4]. In addition, it is possible to measure the sensitivity of ESDS parts when the critical path, charging and handling methods are known in details [8,9].

CBE control requires to use additional measurement methods which are not fully documented. For example, charge analysis are not commonly part of measurement methods done at the manufacturing area. However, combining potential, charge and EMI measurements would enable better control over charged assemblies and other ESD risk locations.

EPS failure sources are most likely the most challenging to prevent and challenging to include in ESD control processes. EPS risks depends on the product type, test system and software used in the system. However, there are some generic rules to follow, such as to limit hot plugging of electronics, which should minimize for example LU damage risks. Naturally, this is not always possible if the system operation need to be tested in an electrical tester in a power on mode. Here a proper system EMC design would be the primary prevention method.

Three example cases are presented in detail to explain how EMI, CBE and EPS risks can be controlled in EPA. These failure cases are also part of the statistics presented in this paper.

A. Defects due to EMI

An electronic testing area had hand held pistol type compressed air assisted ionizers for dust removal and charge neutralization purposes. These ionizers were picked up and product surfaces were blown with ionized air for a couple of seconds. Operators were instructed to keep the ionizer steady, but they typically shook the tool during ionization. These AC type ionizers had two different type of cables in use. The cable included control signal lines, a high voltage wire and an air supply pipe in a single bundle with rubber outer casing.

During the usage the HV cable type *B* inside the bundle became physical damaged around the cable bending areas, as can be seen in Figure 4. The cable and ionizer still operated according to the specification, but the broken cables started to emit EMI pulses due to the sparking between the middle HV wire and a shield conductor. Some of the cables had cracks also along the center conductor. The generated RF noise radiated and coupled into product testers a few meters around the workbench and produced test failures. With some testers the testing failure rate was tens of percent's.

A Sanki EMI Locator tool was used to locate the source of RF noise. The detector was able to sense the broken cables a few meters distance, and by bringing the detector beside the cable, damage locations were seen from the LEDs informing the signal amplitude. The broken cables were tracked also by using an oscilloscope and antennas, and an example measured waveform is shown in Figure 5.

All the HV cables were changed to more robust type *A* and that solved the failure case.

Based on the EMI problems found the company integrated EMI control as a part of the ESD control program. EMI detection was carried out systematically close to the testing, programming and RF measurement equipment. This revealed several new significant EMI and a lot of low amplitude RF noise sources. It would have been difficult to remove all the noise sources. Therefore, to optimize the EMI mitigation new detailed measurement setups and control thresholds were defined. Based on the measurement data and risk analysis only the most relevant EMI sources were removed inside EPA.

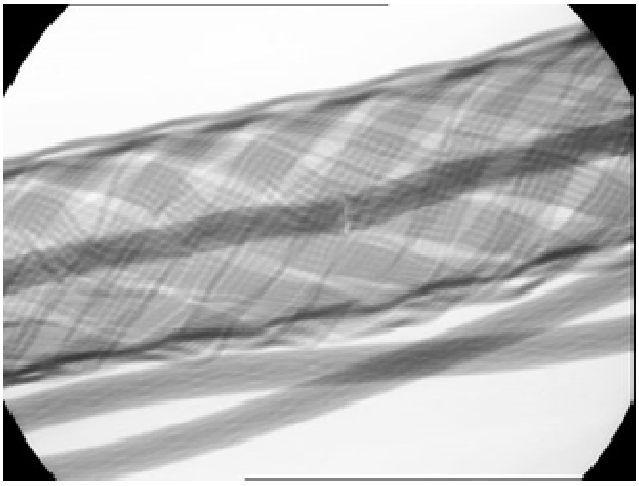

Figure 4: X-ray image of a broken high voltage cable.

B. CBE defect case

An electronic system had a small hard disk drive inside the enclosure. The hard disk was assembled with a rubber cushion material to protect the disk from excess accelerations and shaking. The disk and cushion material is shown in Figure 6.

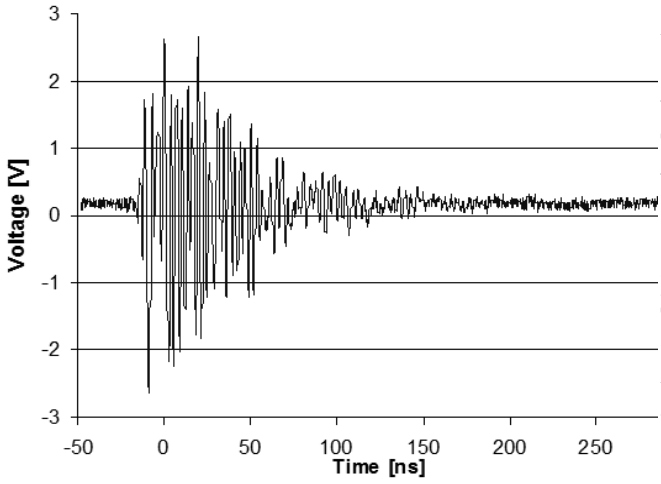

Figure 5: Measured EMI pulse with a monopole antenna.

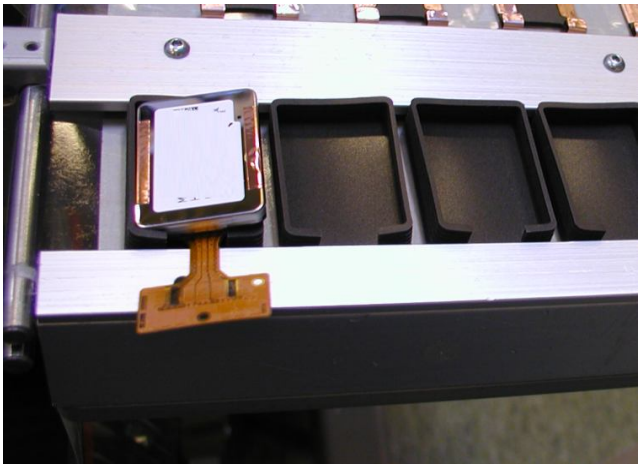

Figure 6: A hard disk and dielectric black color cushion.

Hard disks were found to have electrical failures in a final testing phase and the supplier of the disk reported electrical overstress or ESD damage with control electronics based on failure analysis. The hard disk had reasonably good ESD protection design and was able to withstand ESD up to 4 kV based on IEC61000-4-2 qualification. The enclosure of the disk was conductive and the handling area had all basic EPA precautions in place. However, the cushion material was made of dielectric rubber and got triboelectrically charged when the disk slid inside.

When the operator placed the disk inside the cushion material, he/she grounded the disk via hand and only less than 100 V surface potentials were found on the metallic enclosure of the disk. However, when the assembly was picked up from the feeder the capacitance of the assembly decreased, thus, increasing the static potential over 1 kV. In addition, the measured charge in metal parts of the disk was more than 10 nC. During the next assembly phases the assembly was poorly grounded due to the dielectric cushion material, and therefore, charges of the disk discharged into the main PCB when the flex connector was pressed in place. Random EMI pulses were also detected at the assembly location.

There was an additional ESD risk scenario, which is visible also in the Figure 6. The flex connector was able to touch on the metallic surface of the feeder during handling. This was prevented by adding a piece of dissipative material on the contact area.

The failure case was completely resolved by spraying semi-conductive liquid on the cushion surface prior to the assembly. That reduced charging phenomena until the system was fully assembled. Later on, the dielectric cushion material was replaced with a dissipative version.

In this failure case charge measurement was the primary method together with EMI detection to locate and analyze ESD risks. By using potential or E-field measurements alone the charging phenomena would have easily remained undetected. Therefore, a basic method to detect and analyze similar CBE risks is to use EMI, potential and charge measurements in parallel.

C. Latch up defect case

An electronic system was programmed via USB2 interface before it was packed for shipment. During a dry winter period programming equipment started to suffer electrical failure to a USB control card inside an industrial computer. Only one specific USB card

model showed failures. In a short period of time tens of cards broke, but the products under programming were still fully functional.

The product had a plastic casing and that charged up to a few hundred volts when it was manually handled in the programming phase. This induced around 5 to 10 nC static charge on electronics inside the casing. When a worker plugged a USB cable into the product an ESD discharge went through the cable into the computer as shown in Figure 7. This discharge was relatively weak, but initiated a latch up phenomena in the USB card that led to damage to USB control circuits.

The process phase was measured with electrostatic field meters, EMI detectors and charge meters. There were systematic weak EMI pulses found when the USB cable was plugged in, but voltage or charge values were still well below set alarm limits.

The USB cable used had no extra ferrite bead EMC filtering. In addition, the ground shield of the USB wire was connected only in one end of the cable, thus, all the product charges discharged via the signal pins between the product and the USB card. The USB card had unknown EMC/ESD design and the primary corrective action was to improve EMC/ESD filtering with the data connection. The case was completely resolved by adding two low cost snap-op ferrite cores along the USB cable.

In this failure case the challenge was related to detection of possible ESD/EMC/EPS risks in the process, as only weak EMI pulses indicated problems in the process area. It showed also that even weak ESD or EMI events may trigger latch up or other fatal EPS events. In addition, the victim may not be always the ESDS, but another equipment used in the process area.

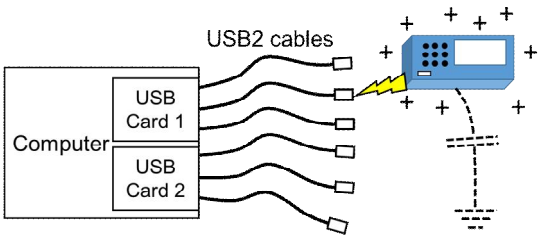

Figure 7: LU failure triggered by an ESD event.

V. Conclusions

ESD control programs are successfully used to prevent most ESD related failures. However, in this study we present statistics of failure cases found in an electronics assembly environment during the last 10 years. All these events have occurred in well controlled EPAs producing industrial, commercial and medical electronics. The purpose of this paper has been to demonstrate how to further improve ESD control programs to cover the most common types of events not currently addressed.

These failure cases are analyzed by categorizing them according to the failure source, event type and parts failing. As well as physical failures we include EMI related disturbances in the study, as these represent a major part of the cases found.

Current ESD control programs are not fully able to detect and prevent CBE and EMI related failures and disturbances. These represent about 70 % of the reported failure sources and around 80 % of the events leading to a product or system failure in electronics assembly environment. In addition to these, there are power source and ESA related challenges.

IC level failure has been proved in about 50 % of the defect cases. The second largest failing group are the electrical testers, programming tools and manufacturing equipment. The failure symptom is typically a system upset but hard failures were also seen.

Only a very few MM, HBM and CDE related events have been observed in this study. This is also related to the type of industry the data has been collected. Most of the products in this study have been computers, consumer electronics and medical systems. Therefore, EPAs with for example automotive electronics manufacturing, semiconductor or back-end processes may have a different failure distribution.

In conclusion, improving CBE and EMI control would be most likely to bring the most benefit for current ESD control programs used in electronics assembly. Here additional measurement methods based on EMI detection and charge measurement are required.

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Characterization of ESD Risks in an Assembly Process by Using Component-Level CDM Withstand Voltage

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Abstract - An effective ESD protection program in electronics manufacturing requires adaptation of CDM withstand information to practical protection actions. Tested withstand voltages differ from the real world discharges, which depends on physical environment and device package. In this study, we will present a calculation method that can be used to assess CDM risks in placement processes.

I. Introduction

A standardised Charge Device Model (CDM) test is used to define withstand voltage of the ESD sensitive device (ESDS). Minimum CDM withstand voltages have been estimated to even further decrease [1]. That's why users of ESD sensitive devices should ensure that the maximum voltage induced on their devices is kept even below 50 volts. However, simulated CDM withstand voltage may not be the same in a practice where discharges may happen in different environments. In addition, a component level CDM withstand voltage is not typically valid anymore when the component is soldered on a PWB.

The standardised CDM discharge test is highly dependent on the device package. Withstand information represents the worst case situation where a single device may have a discharge without damage. The physical environment of CDM testers and the effect of tester construction on CDM stress level have been studied in several papers [2] [4] [5] [5]. However, there is less information available for the typical real world processes where CDM risks may occur in electronics manufacturing [6] [7].

1. Motivation

Component assembly is the most common and often also the only phase of process in electronics manufacturing where the component is handled for a short time as an individual device. Therefore, this is the typical process where CDM withstand voltage would apply. However, due to differences between component assembly and the CDM testing environment the following questions were raised.

- What is the physical environment where the CDM withstand voltage of ESDS is defined?
- What is the physical environment during component assembly and how it differs from the CDM testing environment?
- How the component package affects CDM sensitivity?

These topics should be understood to prevent CDM risks in a component assembly. For this reason, this paper focuses on creating simplified calculation models for the CDM testing and for the assembly environment. The discharge event itself is not studied in this paper. Instead, the target of the calculation is to clarify electrostatic parameters that will affect the initial CDM stress level. The calculations are verified by experimental tests with three different component packages.

2. Scope of the work

This study presents calculation methods that can be used to evaluate the physical environment where CDM discharges may happen. At first, we have clarified calculations for the CDM withstand testing and placement. Those are shortly explained in the next section. In section III the calculations are applied to the standardised CDM test environment and compared to the measurement results obtained with three different component packages. In section IV the calculations are applied to component assembly environment and compared to the measurement results obtained with the same three component packages. In the final sections we summarize the results of the work.

II. Procedure

A. Theory

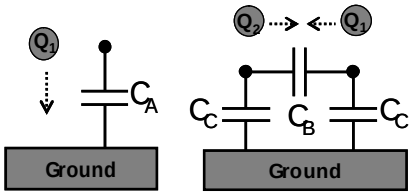
1. Grounding a charged object

Static charge, that is stored on a conductive object, causes potential difference between the object and ground. The higher the initial stored charge is, the higher average electrostatic field densities there are between the object and ground. Finally, the shape of the object and surroundings will define electrostatic field densities that correspond with the charge distributions on the surface [8]. In comparison with planar surfaces, sharp edges or peaks create strong electrostatic fields, and discharges from the charged objects will typically originate from these areas.

When a charged object moves closer to a ground, the field gets stronger and an air or contact discharge will occur. An air discharge may occur before physical contact if the electrostatic breakdown field strength in air (3MV/m) is exceeded. In addition, the Paschen curve can be used to predict the probability for an air

breakdown when the distance between the objects is more than one micrometer. However, when the distance decreases, the capacitance C_A of the object increases and potential approaches zero (ground level), Figure 70a). The decreasing potential reduces both energy and power of the discharge, which reduces the risk of destructive ESD in case of ESDS. If the potential is well below Paschen curve the air discharge may not occur at all.

The shape of the object and ground will specify the capacitive environment before discharge. An equal electrostatic field between the object and ground is needed in order to get high capacitance for the charged object before discharge. In practice, this means that both the object and ground must have flat surfaces which are parallel to each other.



a) b)

Figure 70: Charged objects that are approaching a) ground or b) each others.

2. Connecting two charged objects

When two charged conductive objects are moving closer to each other, the potentials of the objects change due to change of capacitance. Objects are capacitively coupled to ground C_C and each other C_B, Figure 70b). The potential between approaching objects is now a product of the charges and capacitances. If the capacitive coupling is strong just before discharge, the potential difference between the objects may be low, and destructive discharge may not occur.

B. Simulated cases

1. Component assembly

Electronic components typically have dielectric packages and components are electrically isolated during assembly. Depending on the layout and construction of the automated processing equipment, PWBs are also either electrically isolated or grounded via clamping mechanics. Both the component and PWB may have electrostatic charges e.g. due to triboelectric effects or electrostatic induction. These charges may cause CDM type of discharges [6].

Electrostatic field strength and potential between the PWB and Electrostatic Sensitive Device (ESDS) represent severity of an air or contact discharge at the moment of component placement. Therefore, a calculation method is now presented for the simulation of component assembly.

Equations 1 to 6 are used to calculate electrostatic field and potential between ESDS and PWB with a specific component joint height when distance between ESDS and PWB is changing. In the equations it is assumed that the ESDS has an initial static charge Q. Dimensional parameters of the equations are shown in Figure 71 and Figure 72. Capacitances C_1 (between ESDS and ground), C_2 (between PWB and ground), and C_3 (between ESDS and PWB) are calculated according to simplified simulation circuit which is presented in Figure 73.

$$C_{ESDS} = C_1 + \left(\frac{C_3 \cdot C_2}{C_3 + C_2} \right) \qquad (1)$$

$$C_{PWB} = C_2 + \left(\frac{C_1 \cdot C_3}{C_1 + C_3} \right) \qquad (2)$$

$$C_3 = \left(\frac{a_{pins} \cdot \varepsilon_0 \cdot \varepsilon_r}{d_{pins}} \right) + \left(\frac{\left(a_{ESDS} - a_{pins}\right) \cdot \varepsilon_0 \cdot \varepsilon_d}{\left(d_{ESDS} + d_{pins}\right)} \right) \qquad (3)$$

$$V_{PWB} = \frac{Q \cdot C_3}{C_{ESDS} \cdot (C_3 + C_{PWB})} \qquad (4)$$

$$V_{ESDS} = \frac{Q}{C_{ESDS}} \qquad (5) \qquad E = \frac{\left(V_{ESDS} - V_{PWB}\right)}{d_{PINS}} \qquad (6)$$

Where: C_1 is the capacitance between ESDS and ground, C_2 is the capacitance between PWB and ground, C_3 is the capacitance between ESDS and PWB, ε_r is the dielectric constant of air, ε_0 is the permittivity of vacuum, dielectric constant ε_d is a product of the package and air and depends on package type (ε_d>1), d_{ESDS} is the distance between pins and effective metal areas inside of the package, d_{pins} is the distance between pins and PWB, a_{ESDS} is the area of package of ESDS excluding the area of pins, a_{pins} is the area of pins, V_{PWB} is the voltage of PWB at a certain distance from ESDS, V_{ESDS} is the voltage of ESDS at a certain distance from PWB, E is an electrostatic field between the ESDS and PWB. Q is the initial static charge of ESDS.

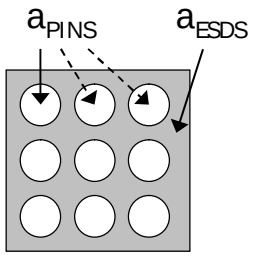


Figure 71: Area dimensions

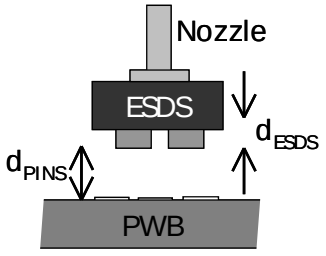


Figure 72: Height dimensions

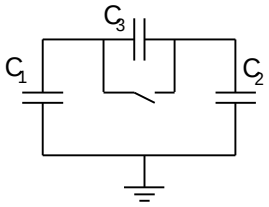


Figure 73: Simplified circuit.

CDM air discharge during assembly can occur when distance between ESDS and PWB is more than a few micrometers. Paschen curve predicts a minimum gap breakdown potential of 330V at a gap of several micrometers and atmospheric conditions. With submicron gaps, Paschen curve will not apply and an air breakdown may still occur [9]. In addition, sharp objects will decrease the minimum gap breakdown potential.

2. CDM withstand test

The environment of the CDM testing is studied in order to verify initial parameters where CDM discharge occurs. CDM tester construction has been presented to effect on the DUT stress level [2] [4]. The stress level depends on the capacitance of the ground plane and pogo pin above the component. The stress level depends also on the capacitance of the induction plate under the component and shape of the pogo pin.

Pogo pin in a CDM tester is at least a few millimeters long. Therefore, distance between induction plate and component body is less than the distance between the component body and ground above the component [5]. This will prevent similar changes to component capacitance just before physical contact when compared to assembly case simulated with equations 1-6.

Capacitances of the DUT can be calculated according to the CDM tester model presented in

Figure 74 and corresponding simplified circuit presented in Figure 75. The DUT has a fixed capacitance between the induction plate and this depends on the thickness of the dielectric layer, thickness of the component package d_p and dielectric constants. The DUT has variable capacitances between the pogo pin and the ground plate above the DUT. The capacitance of the DUT will increase when distance d_G decreases. The induced potential on the DUT can be calculated by using the equation 7. V_{AB} defines the potential that will be induced on DUT at the moment of CDM discharge.

V_{AB} can be used also to calculate electrostatic field between the DUT and pogo pin. However, shape of the pogo pin and joint will effect on the field strength. Therefore, V_{AB} gives only estimation for the field strength that may launch an air discharge. Typically, due to the small diameter of the pogo pin, the field strength is higher at the certain distance than the calculation gives.

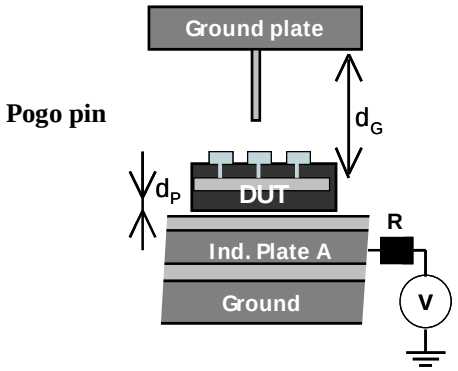


Figure 74: CDM tester

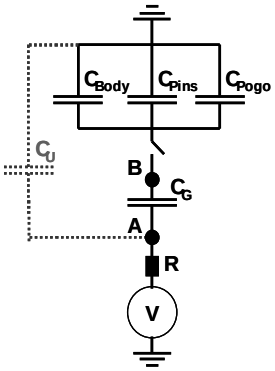


Figure 75: Simplified CDM circuit.

$$V_{AB} = \frac{C_G - (C_{Body} + C_{Pins} + C_{Pogo})}{C_G} \cdot V_{Ind} \qquad (7)$$

Where: C_G is the capacitance between the DUT and induction plate, C_U is capacitance between the induction plate and ground plate above and C_{Body} and C_{Pin} are the capacitances between the ESDS and pogo pin and ground plate above. Capacitance C_U between induction plate and ground above has no effect on the initial situation but will affect the discharge [4].

III. CDM environment

A. Setup

Three component packages chosen for this study are presented in Figure 76 and Figure 77. Land Grid Array (LGA) package on the left has the size of 10mm*12mm*1.67mm. PLCC44 package on the middle has the size of 17.56mm*17.56mm*4.42mm and DIL8 package on the right 6.3mm* 10.3mm*8.36mm. Joint heights with the packages (measured from the bottom surface of the packages) are: LGA = 0.01mm, PLCC44 = 0.42mm, DIL8 = 4.36mm. These Integrated Circuit (IC) component packages represent three dimensional categories that are used in electronics manufacturing. The LGA type

of package is typical with modern high frequency RF electronics where CDM withstand classification is often below 150V.

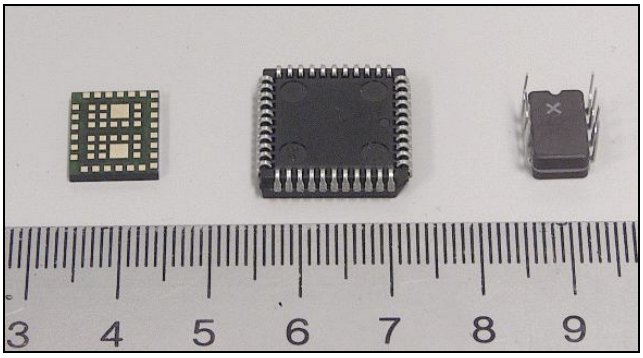


Figure 76: LGA, PLCC44 and DIL8 components used in this study.

Equation 7 is used to calculate potential of the components in a CDM tester environment. Parameters used with the calculation are: initial voltage of induction plate V_{Ind} =1000V, dielectric layer between the LGA and induction plate =0.35mm, dielectric constant of the dielectric layer =4, dielectric constant of LGA and PLCC44 ε_d=1.2, dielectric constant of DIL8 ε_d=2, height of the pogo pin =11mm and area of the pogo pin =1mm^2. Thickness of the component package d_P and length of legs d_{ESDS} are checked with an x-ray system, Figure 77. The measured package thickness d_P is 0.3mm with the LGA, 2mm with the PLCC44 and 1.3mm with the DIL8. Length of legs d_{ESDS} is 0.02mm with the LGA, 1.92mm with the PLCC44 and 6.36mm with the DIL8.

Sharpness of the pogo pin effects the distance where CDM discharge will happen. In this study the pogo pin had an area of cross-section 1mm^2 and a rounded tip. The distance of the air gap between the pogo pin and metal plate was measured after discharge with a clearance gauge. 1000V air discharge occurred when pogo pin had 0.1mm air gap to the induction plate. Therefore, in this study 0.1mm distance is used to predict the distance of CDM event with LGA and PLCC44 components. DIL8 has such a long legs that discharge may occur with longer air gaps.

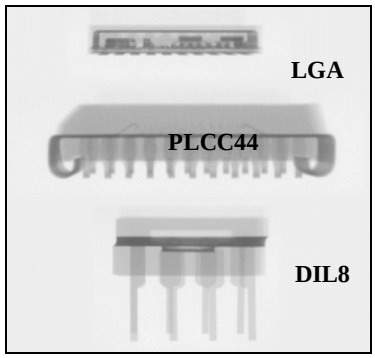


Figure 77: X-ray image of the LGA, PLCC44 and DIL8 packages.

B. Simulated CDM testing

1. LGA, PLCC44 and DIL8 components

From Figure 78 it can be seen that the calculated potential of the LGA decreases slightly when the pogo pin and the ground layer move closer to the DUT. The induced potential of PLCC44 component will decrease close to 900V when the pogo has a distance of about 0.1mm to the component joint. The potential of the DIL8 is about 910V with the same pogo pin distance. Calculated voltage drops before CDM discharges are: LGA V_{drop}<2% and with PLCC44 V_{drop}<9%. DIL8 may have a discharge with over 0.1mm distances and voltage drop can not be predicted exactly. Voltage drop is, however, less than 10%.

The real CDM voltage is less than applied stress voltage. Finally, construction of the CDM tester and type of DUT package defines the voltage drop before air or contact discharge.

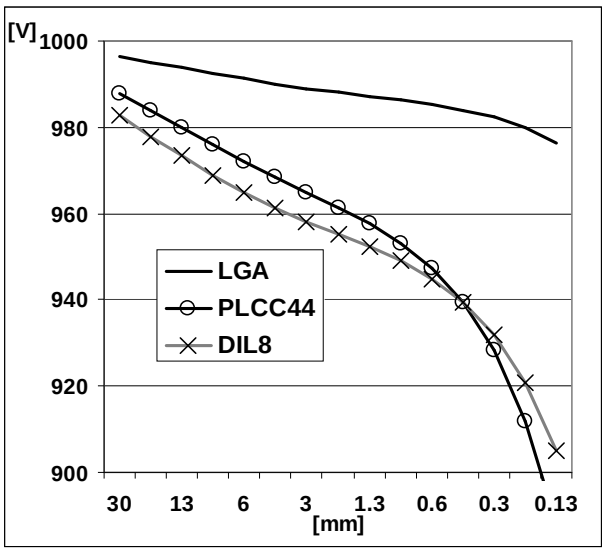


Figure 78: Potential of LGA, PLCC44 and DIL8 components when the pogo pin moves close to component joint

C. Measured CDM testing

1. Measurement setup

Trek370 electrostatic voltage meter was placed to measure potential of the DUT from 2mm distance. An end view type of voltage probe is placed between the induction plate and ground as presented in Figure 79, Length of the pogo pin, thickness of the dielectric layers and components were the same as with the simulated environment in chapter III/B.

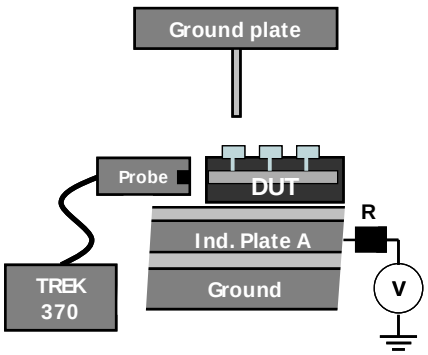


Figure 79: Potential measurement setup

This setup gave us an approximation of the potential of the LGA due to low height of package. PLCC44 and DIL8 packages are sufficiently high to be within that sensing area of the probe. Measurement error for PLCC44 and DIL8 components was below ±30V.

2. Measurement results

Measured potential of the PLCC44 is presented in Figure 80. Initial induced potential of the component on the induction plate was 990V and after approaching the component with a pogo pin a CDM air discharge occurred. At the moment of discharge the measured potential was 940V and distance was about 0.2mm. After discharge the pogo pin connected component to the ground and potential of the PLCC44 was close to zero. Measured CDM potential of the component was approximately the same as the calculated CDM discharge potential 900V shown in Figure 78. Therefore, simulated and measured CDM discharge potentials support each other.

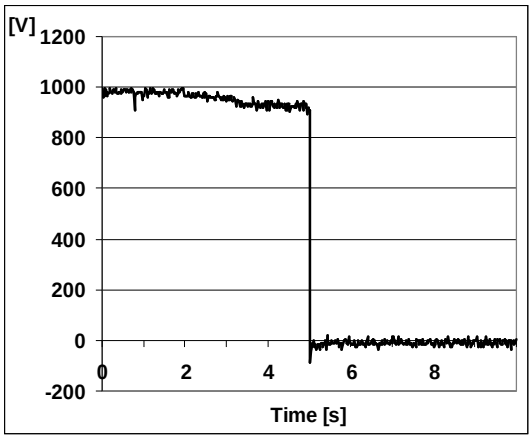


Figure 80: CDM discharge of PLCC44 package

Measured potential of the DIL8 is presented in Figure 81. Initial induced potential of the component on the induction plate was 950V and after approaching the component with a pogo pin a CDM air discharge occurred. At the moment of discharge the measured potential was 940V and the gap of air discharge was more than 0.2mm. The potential of the CDM discharge was also close to calculated potential shown in Figure 78. However, the measured potential did not follow the calculated values exactly due to relatively high component package.

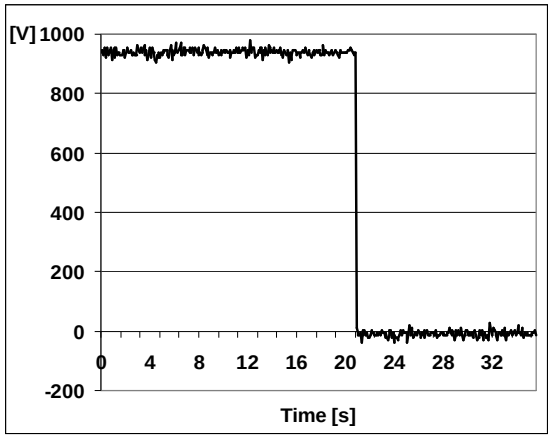


Figure 81: CDM discharge of DIL8 package

IV. Placement environment

A. Setup

The same three components are now used to study CDM discharge environment during component placement. Two cases are simulated: placement of a component on a grounded PWB and placement of a component on a floating PWB.

Equations 1-6 are used to calculate potentials of the DUT and PWB, electrostatic field between the DUT and the PWB, and the potential difference between the DUT and PWB when d_{pins} decreases close to zero.

Parameters used with the calculation are the same as in the chapter III. In these simulations and experiments the DUT has an initial static charge Q and the PWB is either grounded or initially at a zero potential. The thickness of the component package and length of the legs are also the same as used in chapter III.

B. Simulated Placement

1. LGA Component

Component assembly on a grounded PWB is simulated at first. The LGA component has an initial static charge Q=380pC and capacitance C_1=0.36pF. The potential is decreasing according to Figure 82 when the LGA moves closer to the surface of PWB due to increasing capacitance C_{ESDS}. At the same time, the electrostatic field between the objects increases and is about 190kV/m with a distance of 0.1mm. The potential of the LGA, however, is then only about 20V and is less than required to launch an air discharge. Therefore, severe CDM type of air discharges cannot occur with the simulated initial charge level. In order to get over 100V potential difference between the PWB and component, the initial charge of the LGA should be over 5nC. This is not a realistic charge level in the component assembly environment as this would mean over 13000V potential on the component after pick up.

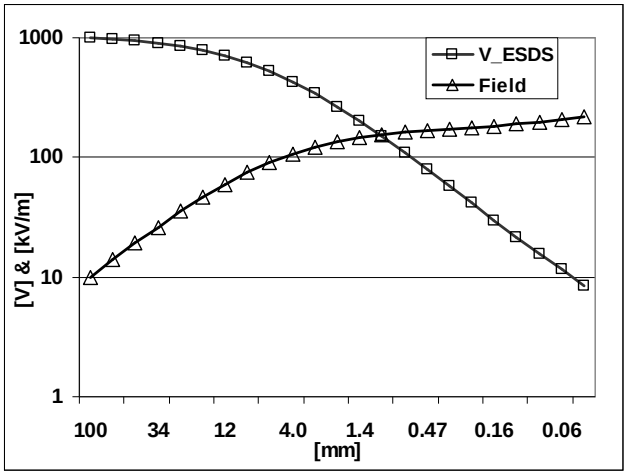


Figure 82: LGA package placed on a grounded PWB.

The same initial charge and capacitance of the LGA is used to simulate LGA assembly on a floating PWB. Now the PWB has an initial capacitance C_2=10pF. According to Figure 83, the potentials of both the LGA and PWB will approach the same value (37V) when the distance between them decreases. V_{CDM} indicates the potential difference between the LGA and the PWB. The electrostatic field between the LGA and the PWB stays well below 3000kV/m and severe CDM type air discharges cannot occur with the simulated charge level.

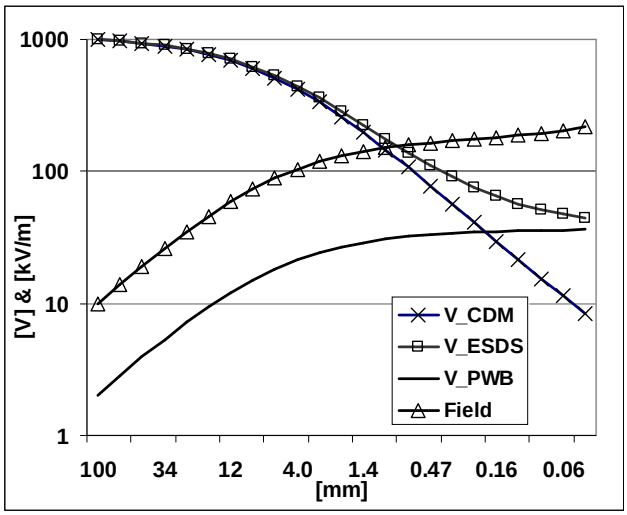


Figure 83: LGA package placed on a floating PWB.

By comparing the CDM test potential of the LGA component in Figure 78 to the placement potentials in Figure 82 and Figure 83, it can be seen that the potential difference is over 900V. The LGA has only insignificant CDM potential in an assembly compared to the high CDM withstand voltage given by the tester. Therefore, CDM withstand voltage does not apply in an assembly environment with LGA type of components.

2. PLCC44 Component

Placement of the PLCC44 on a grounded PWB is simulated at first. The PLCC44 component has an initial static charge Q=800pC and capacitance C_1=0.77pF. The potential is decreasing according to Figure 84 when the PLCC44 moves closer to the PWB. Calculating the electrostatic field strength between the PLCC44 and the PWB is not accurate due to the shape of the PLCC44. The electrostatic field is at least 1000kV/m according to equation 6 with a distance of 0.1mm. The potential of the PLCC44 is then about 120V.

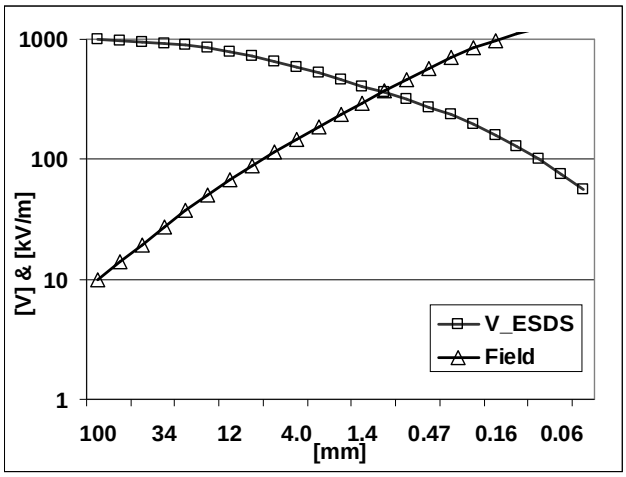


Figure 84: PLCC44 package placed on a grounded PWB.

The same initial charge and capacitance of the PLCC44 is used to simulate the PLCC44 assembly on a floating PWB. The PWB has an initial capacitance C_2=10pF. According to Figure 85, the potential of both the PLCC44 and the PWB will approach the same value (75V) when the distance decreases. V_{CDM} is now about 120V with a distance of 0.1mm.

The potential of the PLCC44 component in Figure 78 differs from the potentials in Figure 84 and Figure 85. It can be seen that the simulated PLCC44 type of component has a much smaller CDM potential level in an assembly environment than in the CDM withstand tester environment. Therefore, CDM withstand voltage does not apply either for the PLCC44 type of packages in an assembly environment. Both the V_{CDM} and electrostatic field values are higher than with the simulated LGA type of package.

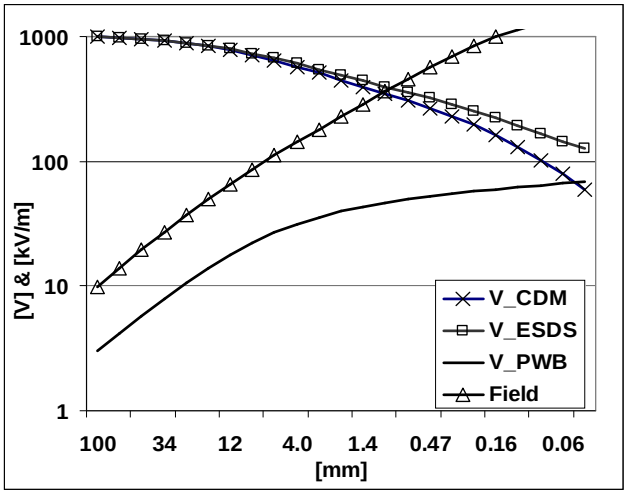


Figure 85: PLCC44 package placed on a floating PWB.

3. DIL8 Component

A DIL8 assembly on a grounded PWB is simulated at first. The DIL8 component has an initial static charge Q=390pC and capacitance C_1=0.39pF. The potential is decreasing according to Figure 86 when the DIL8 moves closer to the PWB. Calculating the electrostatic field strength between the DIL8 and the PWB is not accurate due to shape of the package. The electrostatic field is at least 3000kV/m according to equation 6 with a distance of 0.15mm. The potential of the DIL8 is then about 580V and an air discharge is expected to occur.

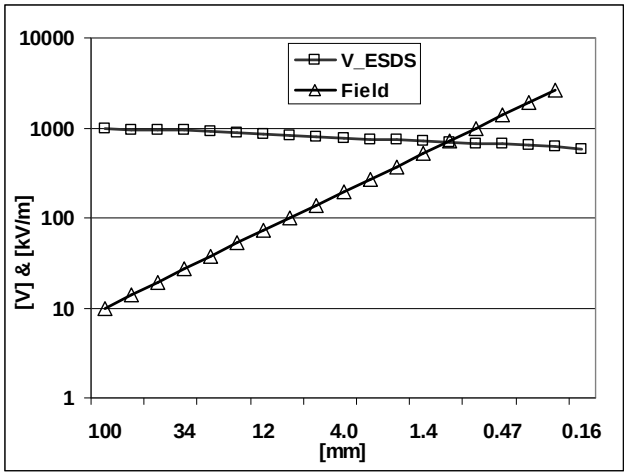


Figure 86: DIL8 package placed on a grounded PWB.

The same initial charge and capacitance of the DIL8 and the PWB are used to simulate the DIL8 assembly on a floating PWB. According to Figure 87, the potential of the DIL8 and the PWB will approach each other, but the effect is weak due to low capacitance between the objects. The electrostatic field is at least 3000kV/m according to equation 6 with a distance of 0.2mm and an air discharge is expected to occur. The potential of the DIL8 is then about 530V.

By comparing the potential of the DIL8 component in Figure 78 and in Figure 86 and Figure 87 it can be seen that the simulated DIL8 has smaller CDM potential level in an assembly environment than in the CDM withstand tester environment. The potential of the device V_{CDM} and minimum electrostatic field values are so high that an air CDM discharge will happen during assembly with the simulated initial charge level.

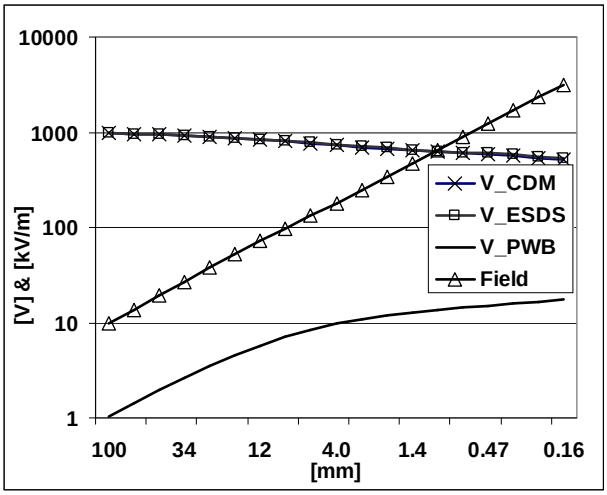


Figure 87: DIL8 package placed on a floating PWB.

C. Measured Placement Environment

1. Setup

Calculated results were verified by measuring the same components in an assembly process. The placement head was simulated by placing the DUT on a metal plate so that the joints were upwards. This represents the situation as shown in Figure 72. The DUT was charged with a HV generator via contact and a TREK 370 voltage meter was used to monitor the potential of the DUT when the PWB moves down on to the component, Figure 88. A loop antenna and an oscilloscope were also used to capture the EMI of the discharge.

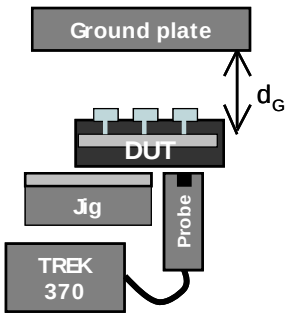


Figure 88: Measurement setup.

2. LGA Component

Measurements with the three components were used to verify calculated results. The LGA component was charged via a contact up to 1450V and a parallel ground plate was moved to 0.2mm distance from the component joints (time: 40s…50s). The potential of the component was then less than 20V as presented in Figure 89. The metal plate was raised up and potential of the component was close to the same as before plate movements. This indicated that there were not air discharges between the ground and LGA due to increase of capacitances. This supports the calculation results shown in Figure 82.

Similar results were obtained by placing a charged LGA on the surface of the ground plate. The initial 1500V potential of the LGA decreased close to 0V without any clear fast drop of voltages. No EMI signal was detected. Therefore, the CDM discharge at the moment of contact is well below 20V.

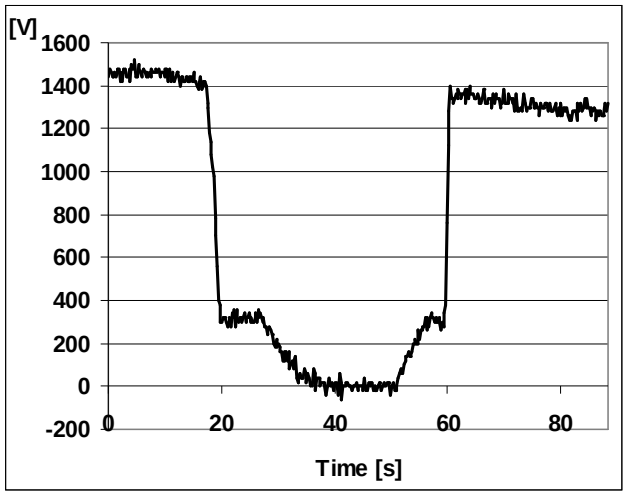


Figure 89: Potential of LGA package.

2. PLCC44 Component

The same potential measurement setup was used for the PLCC44. Now the initial potential of the component after contact charging was 860V. Discharge occurred with about 120V potential and with 0.1mm distance. An EMI signal was also detected. The equations 1-6 give similar potential with 0.1mm distance and 900V initial potential.

3. DIL8 Component

Potential and EMI of the DIL8 were measured. Now the initial potential of the component was 760V and an air discharge occurred with 300V potential. An EMI signal was also detected. Calculation gives about 100V higher CDM discharge potential for the DIL8 package. This is due to high package of DIL8 and capacitances are not calculated as precisely as for the LGA or PLCC44 packages.

V. Conclusion

A CDM discharge event itself is often challenging to predict and measure. Therefore, CDM type of ESD risks are estimated by calculating initial CDM potential of the component before discharge. Three different component packages were evaluated in this study: LGA, PLCC44 and DIL8. Potential of the component is calculated in a CDM withstand tester and in a component assembly environment. Simulated cases are also verified with real word

measurements by using a test setup and real components.

CDM potential depends on the initial charge and capacitance. Capacitances can be calculated by measuring component dimensions and by modeling the surfaces component approaches. When component package has a simple shape, such as with the LGA type, the calculation gives reliable results. High components, such as DIL type of packages, are more challenging to model and calculated CDM voltage will not be as precise.

In a CDM tester environment the CDM voltage drop is less than 10% before discharge with all three package types. When components approach a flat grounded surface, the drop of CDM potential is more than 95% with the LGA, more than 85% with the PLCC44 and about 40% with the DIL8. The drop of CDM voltage between charged component and electrically floating PWB follows closely the same as if component would approach a grounded surface.

Simulations show that CDM risk depends mainly on the component shape and initial static charges stored on the ESDS or the PWB. According to calculations and measurements, the CDM withstand voltage alone is not adequate for estimation of risks in a placement process. The voltage together with information of mobile charge provides a more accurate estimation of risks especially if the dimensions of objects and environment are taken into account.

Simulations can be also used to design the most safe component package type for CDM sensitive devices. From the three tested components LGA is the safest type of package for CDM-sensitive electronics.

VI. Discussion

Calculating the exact capacitances for the component and the PWB would require more sophisticated methods. However, these simplified methods are found to be accurate enough, as calculated and measured CDM potentials followed closely each other. These results already gave answers to the three questions we set in the beginning of the paper.

In this study we did not concentrate on the effect of solder paste during assembly. Paste may be an inhomogeneous and resistive material and may effect on CDM discharges when a charged component is placed on it. The effect of solder paste for CDM discharges in an assembly environment needs still further research.

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Field Collapse ESD Event

Paper 2B.2, EOS/ESD Symposium, 2014.

Field Collapse Event ESD Test Method

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50 Words Abstract - A novel field collapse event ESD test method is presented in this paper. The device under test is continuously grounded in an electrostatic field and when the field is removed it drives current through the device. We show with measurements and simulations how to use this method to test ESD immunity of electronic products

I. Introduction

It is challenging to build up a single ESD stress test method that could represent all possible real life ESD scenarios. Therefore, several test methods have been developed, such as the Human Body Model (HBM), Charged Device Model (CDM), IEC61000-4-2 based immunity tests, and non-standard test methods, such as the Transmission Line Pulse (TLP). It is common for all these methods that they use predefined test setup arrangements and discharge sources during testing. In addition, only TLP method gives detailed measurement data about the ESD stress during the discharge event [1-5].

We also need test methods which can simulate or reproduce certain real world ESD waveforms. A typical need for such a test is during product handling and assembly where we need to know what kind of ESD pulses can disturb or damage products [6,7,8,9]. These discharge events also include cases where the charged component or product itself is the source of discharge and these events can be modeled on a component level with CDM and on a system level with Charged Board Event (CBE) [1,7,8,9,10]. With these two methods the discharge waveform is device dependent and simulates a discharge scenario where the ESD waveform is a step response of the circuit when the charged DUT is grounded. However, CDM uses a standard test setup where the discharge path parameters are fixed [1,8]. CBE can have both fixed or varying discharge path parameters and provides a way to simulate real world discharges with non-grounded products [7,9,10].

In this paper we present a novel way to carry out electrostatic discharge (ESD) immunity testing for electronic products. The Field Collapse Event (FCE) bases on a fast changing electric field which drives current into a device under test (DUT) by induction. The authors have successfully used this method to test ESD immunity of electronic products in cases where the system failure bases on impact of rapidly changing electrostatic field.

This paper presents the theoretical background of the FCE method and shows with two example cases how to simulate and measure DUT stress levels. We will present FCE test method and test setups in Chapter II, compare RLC/2D/3D simulation and measurement results to each other in Chapter III and finally give conclusions in Chapter IV.

II. FCE Test Method

CDM, FCE and CBE base on the same initial setup where the DUT is placed on top of a known dielectric layer which is on a conductive induction plate. The induction plate is electrically floating and is charged up to a selected voltage which creates an electrostatic field around the plate. This field is used to charge the DUT and initiate the discharge event.

FCE can use the same basic setup as CBE or CDM, but there also are major differences between the methods [1,8]. The main difference is that in FCE the DUT is continuously grounded into the test setup ground via one or several wires. In addition, the ESD event is initiated by grounding the charged induction plate. The DUT grounding point, or points, also are the DUT stress points similar to CBE or CDM, but these methods have always only one grounding point.

The main benefits of the FCE method over CDM and CBE are that the DUT is continuously grounded during the discharge, and an air spark is not along the DUT ground path. In addition, DUT can be in a power on state, and it is possible to measure DUT parameters with high impedance current and voltage probes during ESD tests. Discharge waveforms can also be adjusted by varying the test setup dimensions and by varying the discharge path resistance, inductance, and capacitance (RLC) parameters.

FCE don't try to simulate IEC or CDM type of ESD stress [1,4]. Instead, it is targeted to study those scenarios where a charged product discharges via known contact points. One real life example is a case where a charged person holds a tablet computer, and connects an USB or charger cable with the tablet, thus, providing a ground connection for the product.

A. FCE Test Setup

1. Equivalent Circuit

A simplified FCE test setup is presented in Figure 1 and an equivalent circuit for the setup is shown in Figure 2. The current I_{Tot} flowing through the induction plate discharge wire is a sum of two main currents I_1 and I_2. I_{Tot} is a complex waveform as there are three capacitances, two parasitic inductances and two dynamic resistances affecting on the realized current. The DUT discharge current I_1 is the most interesting parameter to monitor, and it can be measured with a current transformer along the DUT ground wire.

The total initial capacitance of the test setup is $C_{Tot} = C_{Ind} + C_{DUT}$. However, DUT has only the capacitance C_{DUT} left when the discharge is initiated by grounding the induction plate with a charge stored in the C_{Ind}. Thereby, the total discharge energy of the event can be adjusted by selecting the potential level, size of the induction plate, and the dielectric material between the DUT and the induction plate. The FCE setup also requires that the physical area of the induction plate is at least the same as the area of DUT, as we need to create a uniform electrostatic field between the DUT and induction plate. However, the capacitance of the induction plate C_{Ind} can also be smaller than C_{DUT} and this gives us interesting options to tailor the discharge waveforms when needed. For example, when C_{ind} /C_{DUT} is smaller than about 1:20, the DUT current I_1 depends mainly on the C_{DUT} , L_{DUT} and R_{DUT}, and can follow more a single frequency underdamped RLC waveform.

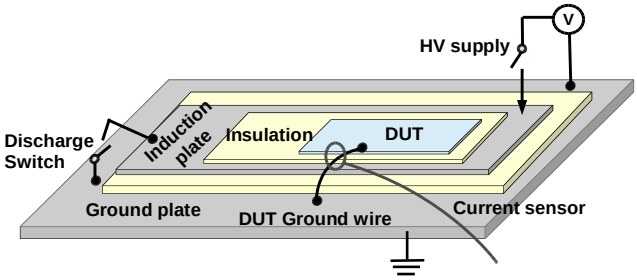

Figure 90: FCE test setup.

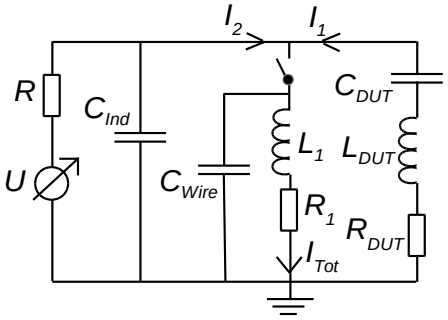

Figure 91: FCE equivalent circuit.

The parasitic capacitance of the ground wire of the induction plate is marked with C_{Wire} in Figure 2, and it can add high frequency oscillations into the current measurement results. On top of that, the DUT ground wire can have a similar parasitic capacitance, but both these capacitances can be omitted when the values are significantly smaller than C_{Ind} and C_{DUT}.

The capacitances C_{Ind} and C_{DUT} can be measured with an RLC meter or those can be calculated from the measured charge and potential value by using an equation $C=Q/V$. The inductance of the induction plate discharge wire L_1, and the inductance of the DUT ground wire L_{DUT}, can also be calculated from the circuit resonance frequencies when the capacitances C_{Ind} and C_{DUT} are known, and the waveform is underdamped.

The charging resistor R in Figure 2 is typically set to >100 MΩ and don't affect on the discharge event. The resistances R_1 and R_{DUT} are the most challenging parameters to set exactly as these depends for example on the discharge voltage, current, and frequency. In addition, R_1 depends highly on the spark resistance. Both resistances affect mainly on the discharge current amplitude and the attenuation of the oscillation. Resistance values can be estimated from the measured current values, if the capacitance and wire inductance values are known. However, simulations can be used to estimate the resistances even easier as presented in the following section.

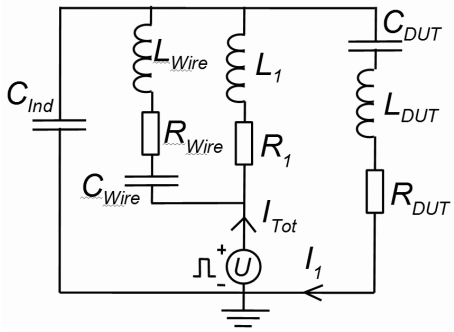

Figure 92: FCE SPICE simulation equivalent circuit.

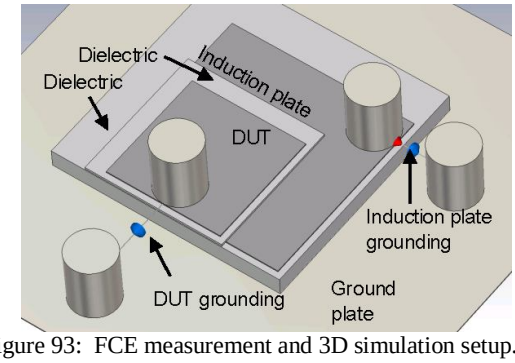

Figure 93: FCE measurement and 3D simulation setup.

2. FCE Simulations

FCE discharge scenarios are simulated with SPICE software tool by using an equivalent circuit shown in Figure 3. It is similar to Figure 2 FCE equivalent circuit, but now the voltage source U gives a step function which will drive current into the capacitors C_{Ind} and C_{DUT}. Simulated current waveforms I_1 and I_{Tot} are compared to the measurement results in Chapter 3.

In addition to SPICE, we use CST Microwave Studio to simulate FCE discharge waveforms, and the simulation 3D model is presented in Figure 4. The DUT and the induction plate sheet materials are modeled as stainless steel, and the dielectrics are modeled as Polytetrafluoroethylene (PTFE). Both the SPICE and 3D simulation base on the RLC network calculations, but 3D tools also can model the DUT and test setup circuit parameters based on the test setup dimensions and used materials.

B. Measurement Setup

Figure 4 shows an experimental FCE measurement setup used in this study. To simplify the measurements and simulations, we use a stainless steel metal plate with a size of 100 mm x 100 mm x 1 mm as the DUT. The size of the stainless steel induction plate is fixed to 160 mm x 160 mm x 1 mm. Both the induction plate and DUT ground wires go through a current transformer so that the discharge currents I_1 and I_{Tot} can be measured. The total inductance of the discharge paths is selected so that the main oscillation frequencies stay under 200 MHz and Tektronix CT2 current transformers can be used. 200 MHz bandwidth limitation will partially filter away high frequency signals which originates from the radiated noise, ground wire and induction plate internal oscillations. It is possible to use faster current transformers, such as Tektronix CT1, but in that case the stress voltages should be kept lower.

The induction plate is connected to a high voltage source via a 10 GΩ resistor. The induction plate is above a large ground layer on top a dielectric sheet. The capacitance of the induction plate C_{Ind} is varied by adjusting the PTFE sheet thickness between 11 mm and 16 mm. The capacitance C_{DUT} is kept constant by using 2 mm thick PTFE sheet between the DUT and the induction plate. The ground wire diameter is fixed to 0.6 mm and two wire lengths 30 mm or 60 mm are used with the example cases. The discharge is initiated by touching the wire on the top right corner of Figure 4 with a grounded metal cylinder beside. The metal cylinders held the ground wires tightly against the metal plates. In addition, the weight of the cylinders press the metal plates and PTFE layers together, thus, improving measurement repeatability. Measurements were made in 22 ºC and 15 ± 3 % RH environment.

III. Test Results

A. Example discharge scenarios

Figure 5 shows both the simulated and measured currents for the first discharge scenario where; C_{Ind} is 50 pF, C_{DUT} is 82 pF, L_1 is 44 nH, L_{DUT} is 26 nH, R_1 is 3.5 Ω, and R_{DUT} is 1.5 Ω. C_{wire} is kept as an open circuit in simulations. The second scenario in Figure 6 has 30 mm long discharge wires and the capacitance of the induction plate is two times higher; C_{Ind} 102 pF, C_{DUT} is 76 pF, C_{wire} is 0.5 pF, L_1 and L_{DUT} are 32 nH, R_1 and R_{Wire} are 2.3 Ω, and R_{DUT} is 1.2 Ω. The initial potential level is 500 V and the capacitance and inductance values are measured from the test setup based on the total charge transfer and resonance oscillation frequencies. The measured currents are averages of 16 discharges and the simulations are made with SPICE.

The DUT current I_{DUT} has an opposite polarity to I_{Ind} and has the same main oscillation frequency 58 MHz. I_{DUT} also has a second higher oscillation frequency 228 MHz based on the two other oscillating RLC networks shown in Figure 2. The simulated currents follow well the measured currents, except during the high frequency oscillations and after 60 ns when the current amplitude already is below 3 A. This difference comes from the oscilloscope and current transformer 200 MHz limitation and from the averaging of the measured currents. In addition, SPICE simulations use fixed resistance values whereas the real life discharge has dynamic resistances [6,8].

3D simulation tools can predict DUT ESD currents without given inductance and capacitance values. The second scenario is simulated with CST Microwave studio based on the setup shown in Figure 4, and the simulated DUT discharge currents are presented in Figure 7. 3D simulation estimates the capacitance and inductance values based on the test setup parameters and only the discharge resistance must be given. The simulated 3D current has slightly different oscillations due to the inductance and capacitance differences, but the discharge current still predicts fairly well the DUT ESD stress level.

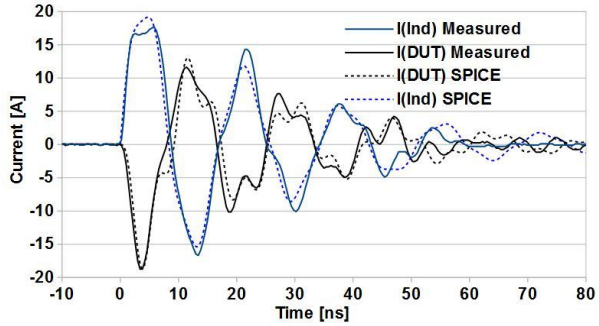

Figure 94: FCE measurement and 2D simulation results for the first discharge scenario.

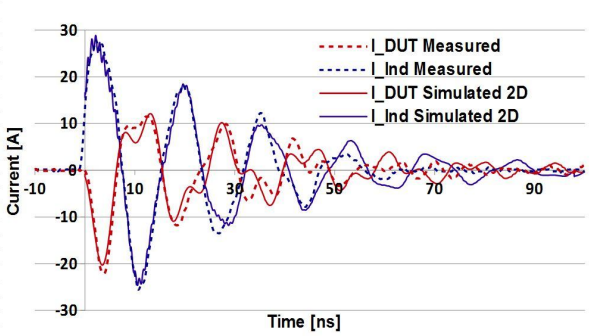

Figure 95: FCE measurement and 2D simulation results for the second discharge scenario.

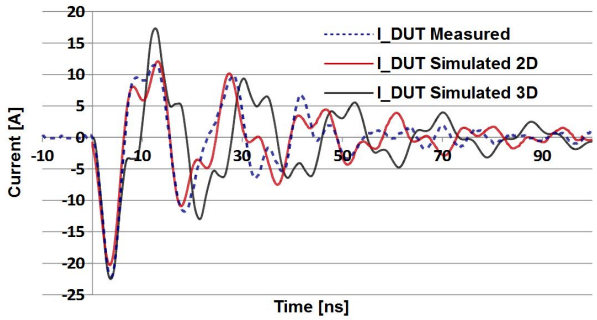

Figure 96: FCE measurement and 2D and 3D simulation results.

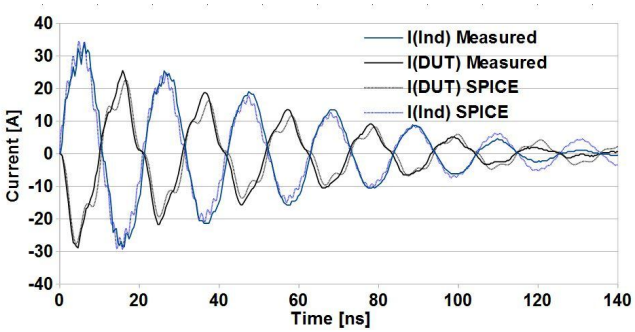

Figure 97: FCE measurement and 2D simulation results for the third discharge scenario.

When the induction plate capacitance C_{Ind} is smaller than the DUT capacitance, and the inductance L_1 or L_2 is higher, the DUT discharge current I_1 starts to follow more an underdamped RLC discharge waveform. Figure 8 shows simulated and measured currents for the third discharge scenario where; C_{Ind} is 40 pF, C_{DUT} is 79 pF, C_{wire} is 0.5 pF, L_1 is 78 nH, L_{DUT} is 30 nH, R_1 is 2.5 Ω, and R_{DUT} is 1 Ω. In this case the measured current value is an average of 64 pulses and the discharge potential was raised up to 1 kV.

In this setup we simulated the high frequency oscillation which is visible during the first 40 ns of the current I(Ind) in Figure 8. The simulated and measured waveforms match well when the resistance values are selected based on the measured current amplitude and attenuation. The resistance values R_1 and R_2 are still in the same range as with the first two discharge scenarios where the potential was 500 V.

B. FCE and CBE discharge waveform comparison

The source capacitance of CBE is a serial capacitance of C_{Ind} and C_{DUT}. In FCE the capacitances C_{Ind} and C_{DUT} are in parallel, which makes the difference between the waveforms. Figure 9 has both the measured and simulated CBE and CFE discharge current waveforms with 300 V charge level based on the test setup used with the first discharge scenario. Thereby, the only difference between the discharge events is the way to ground the DUT or induction plate. CBE has been simulated by using the equations 1 and 2 for an underdamped RLC circuits. The DUT ground wire is used as the discharge wire and the inductance of the wire L_1 is 26 nH.

The peak current is about 1.5 times higher with FCE than with the CBE, the total charge transfer is higher and the oscillation of current continues longer. These discharges were made in 40 % RH environment, and therefore, the discharge path resistance values are significantly higher than in the scenarios 1-4. We have to use R=20 Ω with RLC simulation, and R_1=9 Ω and R_{DUT}=2 Ω with SPICE simulation, to get a match with the measured currents. Based on the results there can be different failure signatures between FCE and CBE, and therefore, it is necessarily to give detailed test setup and environmental parameters when ESD sensitivity of electronics is tested with these methods.

$$I(t) = \sin(\omega t) * \exp\left(\frac{-R}{2L}\right) * \frac{-V}{L\omega} \quad (1)$$

$$\omega = \sqrt{\frac{1}{LC_{ESD}} - \frac{R^2}{4L^2}} \quad (2)$$

, where C_{ESD} is the capacitance of the ESD event, L is the inductance of the discharge path, V is the initial

potential and *R* is the resistance of the discharge path.

C. FCE tests with a mobile phone

A mobile phone with an USB cable and audio wire ground connection is used to demonstrate FCE testing. In this case the phone itself is not affected by the discharge, but the target of the analysis is to study the discharge waveforms seen by the electrical device the cables are connected to. The scenario bases on a real life electrical tester EMI coupling case, where a discharge from a charged mobile phone halted the tester operation.

The mobile phone is in a power on state above a 0.1 mm thick transparent dielectric sheet, and the induction plate with a size of 12x15 cm is directly under this sheet. The induction plate is isolated with 2.5 mm thick dielectric from the large ground plane. The USB wire is 140 cm long and the audio wire is 60 cm long. Both wires are set along a table surface far from any ground plane and the discharge currents through the wires are measured with one Ohm shunt resistors by using 500 MHz oscilloscope. The test setup is presented in Figure 10 and the discharge current waveforms are presented in Figure 11.

The induction plate is charged up to 1 kV potential and is grounded via 2 mm long ground connection. The discharge current is higher through the USB cable and based on this information the disturbance case was solved by adding a ferrite bead on the tester USB signal lines.

The same mobile phone test setup was used to study repeatability of the test method. The discharge was repeated 20 times by grounding manually the induction plate with 1 kV charge potential. All the 20 waveforms are presented in Figure 11 for the discharges from the audio wire. The first peak of the current waveform varies so that the average is -3.6 A and the standard deviation is 0.42 A. This variation is mainly coming from the varying manual grounding and from the variation of air spark resistance.

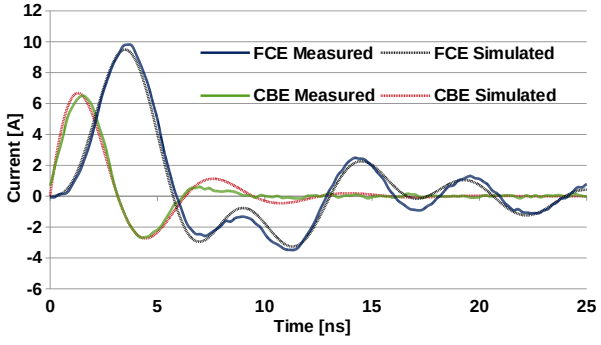

Figure 98: Measured and simulated CBE and FCE discharge currents with 300 V.

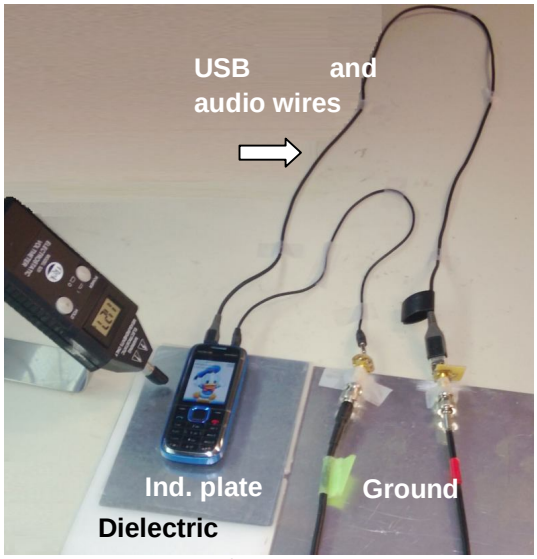

Figure 99: FCE test setup for a mobile phone with two ground connections.

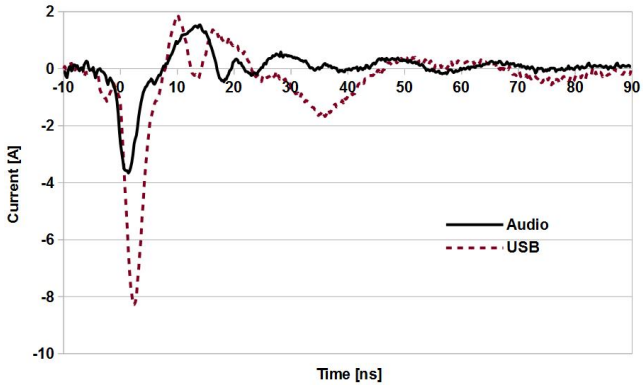

Figure 100: FCE discharge currents between the ground plate and USB and audio cables with 1 kV stress level.

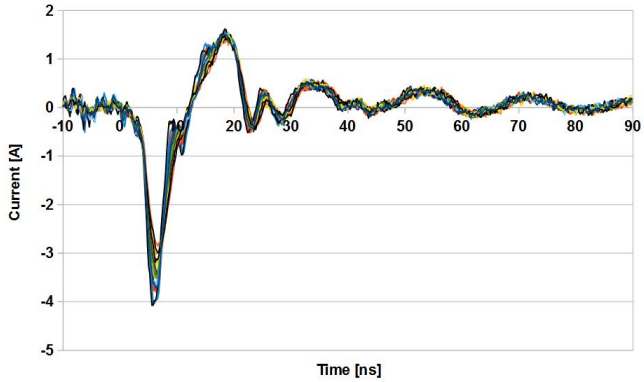

Figure 101: Measured currents of 20 FCE discharges.

IV. Conclusions

In this paper we present a novel Field Collapse Event (FCE) test method for ESD sensitivity and immunity testing of electronic products. FCE represents ESD scenarios where a sudden change in electrostatic field will drive current through a product with one or several ground connections. Tests can be made for

products in operating mode and the test results can be classified in terms of the loss of function or degradation of performance as used in IEC61000-4-2 qualification. With this method it is also possible to measure coupled transients differentially from the signal lines inside DUT during the ESD event.

In the FCE test method the DUT with a fixed ground or power line connection is placed above a charged induction plate. When the charged induction plate is grounded, the fast collapsing electrostatic field will drive current through the product ground connections. The ESD event can be measured with a current transformer, and the charge and energy of the event can be integrated from the measured waveforms.

We also show that the DUT stress current waveforms can be predicted by using SPICE or 3D electromagnetic simulation tools. Simulations also provide information to build up and fine tune the practical FCE test setup. The FCE test setup can vary based on the simulated discharge scenario, and therefore, it is necessarily to specify all the test setup parameters when reporting the test results.

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